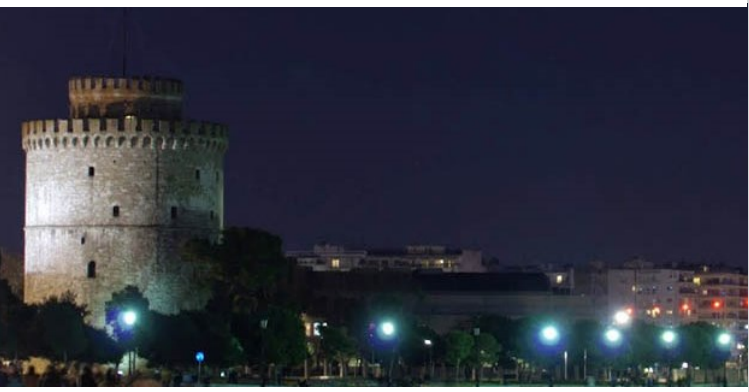
MOCAST

International Conference on

Modern Circuits And Systems Technologies.



Thessaloniki, 7 - 9 May 2018

Conference Guide

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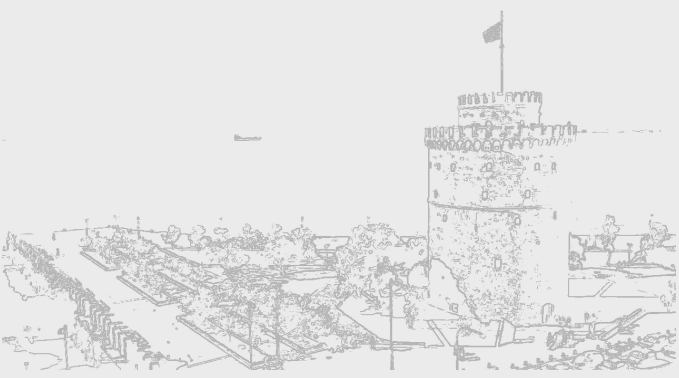
About MOCAST

The International Conference on Modern Circuits and Systems Technologies (MOCAST) on Electronics and Communications aims to bring together leading academic and industrial scientists and researchers to exchange and share their knowledge and experiences about all aspects of Circuits and Systems. It also provides a forum for exchanging ideas, discussing research results, and presenting practical applications in the areas of modeling, design, simulation, synthesis and implementation of Circuits and Systems. It provides an interdisciplinary and multidisciplinary forum for researchers, engineers and educators to present and discuss the most recent innovations, trends, and concerns, practical challenges encountered and the solutions adopted in these fields.

MOCAST takes place in Thessaloniki, Greece. Thessaloniki sits in north Greece in a city which never doubted its own cultural identity and its millennia of existence, it stands there since 315BC. Historically one of Europe's oldest and most multiethnic cities, Thessaloniki is home to architectural marvels that testify to its centrality in Byzantine, Ottoman and Sephardic Jewish history. The city is anchored by Aristotelous Square, where curved, columned facades open to the waterfront in one direction and frame views of the historic Ano Poli (Upper City) in the other. Though it has only about one million people, compared with Athens' five million, Salonika is widely considered the cultural capital of Greece. Thessaloniki is truly unique in the sense that it intricately marries its thousands-year-old multicultural heritage with cutting-edge art performances and cinematic avant-garde.



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Keynote & Invited Speeches, Tutorials

Keynote Speech 1:

The next step in heterogeneous computing: Near-memory and in-memory computing.

Prof. Dietmar Fey, Univ. Erlangen-Nuremberg, Germany

Abstract: The most driving force in designing new processor and computer architectures in the last two decades was the necessity to save the energy consumption in the circuits needed for processing, storing and transporting data. More and more powerful embedded devices as well as manageable HPC systems could satisfy the demand for more compute performance only since they reduced drastically their energy consumption. This process brought us the development from single-core to multi-core and heterogeneous architectures and it is necessary that this process has to continue.

This next step will bring us the realization of new concepts for a closer co-operation of processing and storage into what is denoted as near-memory processing and in-memory processing. This new kind of processing or pre-processing, is the consequence of the fact that it costs sometimes more energy to move data from storage to processor than to process it directly on that location where the data is, either in the memory or close to a data capturing sensor. The last scenario corresponds to edge computing.

The emerging of new memristive devices like e.g. ReRAMs, PCRAMs or STT-MRAMs, which can not only store data energy-efficient but also process it supports decisively the design and future realization of new energy-aware near-and in-memory computing architectures. Besides, they offer also new qualitative benefits compared to conventional SRAM and DRAM technologies like the storage of multiple states in one physical memory cell. The keynote will present a generic overview of the development towards near- and in memory computing concepts as well as an evaluation of concepts for Boolean data processing with memristive devices. In addition, results achieved in the lab of the speaker for energy-efficient non-volatile flip-flops as well as ternary compute units are discussed as a possibility on the way to energy-saving near-memory and in-memory computing architectures.

Short CV: Prof. Dr.-Ing. Dietmar Fey holds a diploma degree in Computer Science from Friedrich-Alexander-University (FAU) Erlangen-Nürnberg, Germany. In 1992 he received a Ph.D. from FAU with a work on an investigation about Using Optics in Computer Architectures. From 1994 to 1999 he researched at Friedrich-Schiller-University Jena where he made his habilitation. From 1999 to 2001 he worked as lecturer at University Siegen before he became a Professor for Computer Engineering at University Jena. Since 2009 he leads the Chair for Computer Architecture at FAU Erlangen-Nürnberg.

Prof. Fey was involved in several national and international research projects and initiatives on parallel and embedded computing. He participated in the nationwide priority Program “SPP 1188 Organic Computing” funded by German Research Foundation (DFG) and in the DFG-funded Ph.D. student elite Research Training Group on “Heterogeneous Image Systems”. Furthermore he was involved in the project “Interchip Optical Communications and Photonic PCBs for next generation OBP” funded by ESA and in joint projects with industrial partners on Grid and Cloud Computing technology. Currently he is a member of the H2020 project AllScale working on new C++ based parallel programming concepts for heterogeneous architectures. He has published over 115 conference papers articles, 3 books, and about 100 papers in journals and reports. He is a member of HiPEAC and a contributor of the HiPEAC roadmap, author of the Eurolab4HPC report “Disruptive Technologies for years 2020-2030”, and he is a member of the EU Cost Action 1401 “Memristors Devices, Models, Circuits, Systems and Applications”.

His research interests are in parallel computer architectures, parallel programming environments, parallel embedded systems, and memristive computing.

Keynote Speech 2:

Dealing with Complexity in Synthesizing System and Devices for Communication/Sensing Systems: The System-by-Design Paradigm

Prof. Andrea Massa, IEEE Fellow, Univ. of Trento, Italy

Abstract: Synthesizing modern devices and systems for Communications and Sensing is mainly concerned with the solution of high-complexity problems, where the term complexity stands for large scale and/or strong non-linearity and/or ill-posedness. Moreover, the focus of the research in the design of complex systems has recently shifted from ad-hoc strategies based on the designer experience to automated iterative search methods thanks to the availability of huge computational resources and by the existence of efficient simulation tools that reliably evaluate the “quality” of the guess design. Nevertheless, several synthesis problems still remain computationally intractable. However, such a class of problems is becoming more and more important because of increasing demand for advanced systems operating across different scales . The SbD is “a functional ecosystem to handle complexity in the design of large systems” and it consists in a guideline for the task-oriented design, definition, and integration of system components to yield devices/systems with user-desired performance having the minimum costs, the maximum scalability, and suitable reconfigurability properties. More specifically, it addresses three fundamental issues. Firstly, the identification of the solution descriptors that represents a formulation challenge. Indeed, a proper choice must guarantee a large flexibility for the potential solution without yielding to huge search spaces, which can become practically unmanageable for any search strategy. Secondly, the evaluation of the system/device response of the iteratively identified guess solutions in an accurate and fast way represents a modeling challenge. The assessment of the effectiveness/quality of a guess design (e.g., in terms of a suitable “cost function”), which is the fundamental information required by any synthesis procedure, should be done efficiently to enable the adoption of automatic iterative search techniques. Thirdly, the choice of the search methodology, which represents an exploration challenge. Actually, the solution-space sampling should find the “best solution” descriptors whatever the complexity of the cost function at hand. Unfortunately, no general purpose approach exists to address these issues and sub-optimal strategies are often adopted in practice. As a result, the SbD guideline is that of defining, through a suitable formulation/re-formulation of the complex synthesis problem at hand, a suitable “environment” for global optimization in which new or re-customized evolutionary optimization tools can perform in a time-effective and reliable way.In order to assess the effectiveness and the reliability of the SbD, several different electromagnetic engineering applications will be addressed as benchmark examples ranging from large radome profiling, complex radar systems, 2D and 3D metamaterial-enhanced devices, as well as other field manipulating devices with potentials at microwave, THz, and optical frequencies. Of course, the intrinsic multi-disciplinary nature and the generalityof the SbD framework also enable its further exploitations in contiguous engineering areas (including acoustics, mechanics, and civil engineering).

Short CV: Andrea Massa (IEEE Fellow, IET Fellow, Electromagnetic Academy Fellow) received the "laurea" degree in Electronic Engineering from the Univ. of Genoa, Italy, in 1992 and Ph.D. degree in EECS from the same university in 1996. From 1997 to 1999, he was an Assistant Professor of Electromagnetic Fields at the Department of Biophysical and Electronic Engineering (Univ. of Genoa). From 2001 to 2004, he was an Associate Professor at the Univ. of Trento. Since 2005, he has been a Full Professor of Electromagnetic Fields at the Univ. of Trento, where he currently teaches electromagnetic fields, inverse scattering techniques, antennas and wireless communications, wireless services and devices, and optimization techniques.

At present, Prof. Massa is the director of the network of federated laboratories "ELEDIA Research Center" (Brunei, China, Perù, Japan, France, Czech, Italy, Tunisia). Moreover, he is Adjunct Professor at Penn State University (USA), Professor at Centrale Supélec (France), and UC3M-Santander Chair of Excellence at the Universidad Carlos III de Madrid (Spain). He has been holder of a Senior DIGITEO Chair at L2S-Centrale Supélec and CEA LIST in Saclay (France), Visiting Professor at the Missouri University of Science and Technology (USA), the Nagasaki University (Japan), the University of Paris Sud (France), the Kumamoto University (Japan), and the National University of Singapore (Singapore). It has been appointed IEEE AP-S Distinguished Lecturer (2016-2018).

Prof. Massa serves as Associate Editor of the "IEEE Transaction on Antennas and Propagation" and Associate Editor of the "International Journal of Microwave and Wireless Technologies" and he is member of the Editorial Board of the "Journal of Electromagnetic Waves and Applications", a permanent member of the "PIERS Technical Committee" and of the "EuMW Technical Committee", and a ESoA member. He has been appointed in the Scientific Board of the "Società Italiana di Elettromagnetismo (SIEm)" and elected in the Scientific Board of the Interuniversity National Center for Telecommunications (CNIT). He has been appointed in 2011 by the National Agency for the Evaluation of the University System and National Research (ANVUR) as a member of the Recognized Expert Evaluation Group for the evaluation of the researches at the Italian University and Research Center for the period 2004-2010. Furthermore, he has been elected as the Italian Member of the Management Committee of the COST Action TU1208 "Civil Engineering Applications of Ground Penetrating Radar".

His research activities are mainly concerned with inverse problems, analysis/synthesis of antenna systems and large arrays, radar systems synthesis and signal processing, cross-layer optimization and planning of wireless/RF systems, semantic wireless technologies, system-by-design and material-by-design, and theory/applications of optimization techniques to engineering problems.

Prof. Massa published more than 600 scientific publications among which about 300 on international journals and more than 450 in international conferences where he presented more than 150 invited contributions. He has organized more than 70 scientific sessions in international conferences and has participated to several technological projects in the European framework as well as at the national and local level with national agencies .

Keynote & Invited Speeches, Tutorials

Invited Speech 1:

Connecting the Dots: A Big Data Paradigm!

Dr. Calliope-Louisa Sotiropoulou, INFN Pisa, Italy

Abstract: We live in the era of "Big Data" problems. Massive amounts of data are produced and captured and require significant amounts of filtering to be processed in a realistically useful form. An excellent example of a "Big Data" problem is the data processing flow in High Energy Physics experiments, such as the ATLAS detector in CERN. In the LHC, 40 million collisions of protons take place every second, which is about 15 trillion collisions/year. For the ATLAS detector, 1 MB of data is produced for every collision or 2000 TB/yr. Therefore, what is needed is a very efficient real-time trigger system to filter the collisions and identify the ones that contain "interesting" physics for processing. The trigger system "connects the dots" to find patterns that are useful.

To achieve the required levels of performance we have constructed the Fast TracKer system. The Fast TracKer is a real-time pattern matching machine able to reconstruct the tracks of the particles in the inner silicon detector of the ATLAS experiment in less than 100 μsec. It is made of 8 different types of custom designed boards with 8000 ASICs and 2000 FPGAs. But this is not enough! We are already preparing the next upgrade, the Hardware Track Trigger, that will provide better performance and efficiency for 2024. All this know-how and high performance hardware can be exploited for a vast variety of applications. We explore implementations on biomedical imaging and security and we have a look on how we can use the HEP hardware accelerators for machine learning and cognitive image processing. We "connect the dots" not only to find patterns but also to find opportunities for new implementations through multidisciplinary research.

Short CV: Dr. Calliope-Louisa Sotiropoulou (IEEE Member '03), holds a degree in Physics and a MSc in Electronics from Aristotle Univ. of Thessaloniki (AUTh). She received her PhD in 2014 (AUTh) in Embedded System Design. After her PhD she received a Marie Curie IAPP scholarship from 2015 to 2017 with the Univ. of Pisa. In 2017 she received a "Galileo-Galilei" Post-Doctoral fellowship and an INFN National Scholarship for Post-Doctoral Research. She is currently a research fellow in the Istituto Nazionale di Fisica Nucleare (INFN), Pisa Section.

Her research lies in the area of advanced image processing implementations and FPGA design. She is working on image processing algorithms and hardware used for particle tracking in High Energy Physics experiments and their adaptations for use in industrial applications. She has been one of the main electronics systems developers of the Fast TracKer project since 2013. She is currently responsible for the FPGA system development of the PRM board for the new ATLAS detector Trigger upgrade and the AM Board of the Fast TracKer system. Additionally, she has been the leader of a group working on an approach on cognitive image processing. This technique mimics the visual functions of the brain and can execute fast contour identification after a learning process that resembles the one used for particle tracking experiments.

She has participated in several European and nationally funded projects and has more than 300 publications (h-index 30). She has been awarded the first prize for best presentation sponsored by Elsevier (NIM) for "A High Performance Multi-Core FPGA Implementation for 2D Pixel Clustering for the ATLAS Fast TracKer (FTK) Processor" in TIPP 2014. She was also selected and participated in the 3rd Heidelberg Laureate Forum. Dr. Sotiropoulou is an academic editor for the MDPI Applied Sciences Journal and reviewer for several IEEE Trans. and other journals. She has organized and has been a member of the organizing committee of 13 conferences and special sessions. She is also an expert project reviewer for the European Commission.

Keynote & Invited Speeches, Tutorials

Invited Speech 2:

Fiber as key enabler for 5G deployments

Abstract: Mobile Networks Evolution demands for significant capacity enhancements as we move from present generation technologies (4G, LTE+) towards 5G.

Fiber, with its ability to offer nearly limitless bandwidth, will therefore become the key enabler that will unlock 5G's potential.

In the new networks, fiber will become the most appropriate medium not only for the backhaul domain (as was the case till now), but also in the front haul.

This is because beyond capacity, fiber can also offer higher reliability, security and resilience vs. other transmission means.

Short CV: Thanos Mantzoros is presently working at Victus Networks, holding the position of "Transport Technologies & F/O Networks Manager". He has more than 25 years of experience in the combined Telecoms/IT domain and more than half of these working within the Mobile Operator Business sector. Also, he has gained significant experience dealing with Fiber & Copper Networks in Greece & abroad.

Thanos is a lifelong member of IEEE and Technical Chamber of Greece and holds an Electrical & Electronic Engineer's degree from NTUA with distinction.

Tutorial:

Converged Optical-Wireless Networks: an Effective Solution for 5G Network Architectures.

John Vardakas, Ph.D., Senior Researcher, Iquadrat Informatica S.L., Barcelona, Spain

Christos Verikoukis, Ph.D., Fellow Researcher, Telecommunications Technological Centre of Catalonia, Spain

Abstract: Converged optical-wireless network architectures can be considered as practical solutions that are able to realize an efficient 5G network for high-density and high-coverage network deployments. This tutorial aims to present a comprehensive overview of current converged optical-wireless networking solutions and to put into perspective their role as promising fronthaul configurations that can provide the means for achieving the demanding 5G requirements. Specifically, the tutorial will cover both the current and future optical and wireless networking schemes, while while highlighting those configurations that are applicable for 5G implementations. Furthermore, converged optical-wireless networking configurations will be presented, while special attention will be given to network management and resources allocation schemes. Finally, research efforts on the application of converged network solutions for 5G fronthauling will be discussed in detail, where data and control planes of the converged fronthaul solutions will be covered, as well as challenges that are related to network components and management functions.

John Vardakas received the Dipl.-Eng. degree in electrical and computer engineering from Democritus Univ. of Thrace, Greece, in 2004 and the Ph.D. degree from the Univ. of Patras, Greece in 2012. He is currently a Senior Researcher with Iquadrat Informatica, Spain. He has published more than 80 papers in journals and international conferences. Dr. Vardakas has participated in more than 12 competitive projects. He is also a regular reviewer in a number of international journals and conferences, while he has participated in the organization of several conferences. His research interests include performance analysis and simulation of communication networks and smart grids. Dr. Vardakas is a member of the IEEE, the Optical Society of America, and the Technical Chamber of Greece.

Christos Verikoukis got his Ph.D. from the Technical University of Catalonia in 2000. He is currently a Fellow Researcher at CTTC and an adjunct professor at Barcelona University. He has published 118 journal papers and over 185 conference papers. He is also co-author in 4 books, 18 chapters in different books and he has filled 2 patents. He has supervised 15 Ph.D. students and 5 Post Docs researchers since 2004. Dr.Verikoukis has participated in more than 30 competitive projects while he has serve as the Principal investigator in national projects in Greece and Spain. He served as the technical manager of the ITNGREENET and the CELTIC-GREEN-T and LOOP projects. Dr.Verikoukis received the best paper award of the Communication QoS, Reliability & Modeling Symposium (CQRM) symposium in the IEEE ICC 2011 & ICC 2014 conference, of the Selected Areas in Communications Symposium in the IEEE GLOBECOM 2014 conference, of the EUCNC 2016 conference and the EURASIP 2013 Best Paper Award for the Journal on Advances in Signal Processing. He was the general Chair of the 17th, 18th and 19th IEEE Workshop on Computer-Aided Modeling, Analysis and Design of Communication Links and Networks (CAMAD), and the TPC Co-Chair of the 15th IEEE International Conference on eHealth Networking, Application & Services (Healthcom) and the 7th IEEE Latincom Conference. He has also served as the symposium co-chair of the CQRM symposium in the IEEE ICC 2015 & 2016 conference. He is currently the Chair of the IEEE ComSoc Technical Committee on Communication Systems Integration and Modeling (CSIM).

Monday, May 7th

08:30-09:00	**Registration**
09:00-09:30	**Opening Session**
09:30-10:30	**Keynote Speech 1** **The next step in heterogeneous computing: Near-memory and in-memory computing.** **Keynote Speaker: Prof. Dietmar Fey, Univ. Erlangen-Nuremberg, Germany** **Chair: Prof. Spiros Nikolaidis.**
10:30-11:00	**Coffee break**
11:00-12:30	**Session A1: Systems and Applications I** **Session Chair: Prof. Konstantinos Tatas**
	Prediction of chaotic time series by using ANNs, ANFIS and SVMs. Ana Dalia Pano-Azucena, Esteban Tlelo-Cuautle and Sheldon X.-D. Tan INAOE, Mexico
	Development of a Cloud-Based Automatic Irrigation System: a Case Study on Strawberry Cultivation. Ercan Avşar, Kurtuluş Buluş, Mehmet Ali Sarıdaş and Burçak Kapur Çukurova University, Turkey
	Driving and Controlling of Blue-Beam Laser Diodes. Kai-Jun Pai Ming Chi Univ. of Technology, Taiwan
	Hardware Optimization Methodology of Multi-Step Look-Ahead Sigma-Delta Modulators. Nick Temenos, Charis Basetas and Paul Sotiriadis National Technical University of Athens, Greece
	A Portable Image Processing Accelerator using FPGA. D. Tsiktsiris, D. Ziouzios and M. Dasygenis University of Western Macedonia, Greece
11:00-12:30	**Session B1: Communication systems** **Session Chair: Dr. Georgios Koudouridis**
	LTE Measurements for Flying Relays Michael Batistatos, George Tsoulos, Dimitra Zarbouti, Georgia Athanasiadou and Sotirios Goudos University of Peloponnese, Greece

Monday, May 7th	
	Joint Network Density and Spectrum Sharing in Multi-Operator Collocated Ultra-Dense Networks Georgios Koudouridis and Pablo Soldati Huawei Technologies Sweden, Sweden
	An Energy Efficient Modulation Scheme for Body-Centric Nano-Communications in the THz band Apostolos Vavouris, Foteini Dervisi, Vasilis Papanikolaou and George Karagiannidis Aristotle University of Thessaloniki, Greece
	Characterization of Second-Order Fading Statistics of 28GHz Indoor Radio Propagation Channels Sardar Muhammad Gulfam, Syed Junaid Nawaz and Konstantinos Baltzis COMSATS Inst. of Information Technology, Pakistan
	Data Representation and Hardware Aspects in a Fully-Folded Successive-Cancellation Polar Decoder Christos Andriakopoulos and Vassilis Paliouras University of Patras, Greece
12:30-13:40	**Light lunch**
13:45-15:15	**Session A2: Modeling, Simulation and Power Management** **Session Chair: Prof. Minas Dasigenis**
	Misalignment-Aware Delay Modeling of Narrow On-chip Interconnects Considering Variability Amir Najafi, Lennart Bamberg, Ardalan Najafi and Alberto Garcia-Ortiz ITEM institute, University of Bremen, Germany
	A Parallel Iterative Approach for Efficient Full Chip Thermal Analysis George Floros, Konstantis Daloukas, Nestor Evmorfopoulos and George Stamoulis University of Thessaly, Greece
	Effective accuracy estimation and representation error reduction for stochastic logic operations. Oscar Camps, Stavros Stavrinides, Rodrigo Picos, Carol de Benito and M. Moner Al Chawa Universitat de les Illes Balears, Spain

Monday, May 7th	
	Large Scale Circuit Simulation Exploiting Combinatorial Multigrid on Massively Parallel Architectures. D. Garyfallou, N. Evmorfopoulos and G. Stamoulis. University of Thessaly, Greece
	Electrical Impedance Tomography Image Reconstruction for Adjacent and Opposite Strategy using FEMM and EIDORS Simulation Models. Christos Dimas and Paul Sotiriadis National Technical University of Athens, Greece
13:45-15:15	**Session B2: Special Session on Wearable Sensor Systems** **Session Chairs: Prof. Gianluca Traversi, Univ. of Bergamo, and Prof. Sergio Saponara, Univ. of Pisa, Italy**
	Development of a telemedicine-oriented gait analysis system based on inertial sensors Andrea Pedrana, Daniele Comotti, Patrick Locatelli and Gianluca Traversi University of Bergamo, Italy
	Carbon nanotubes textile coating for the development of wearable sensors V.Trovato, G. Rosace, C. Colleoni, A. Pedrana, V. Re, G. Traversi, M. R. Plutino and C. Milone. University of Bergamo, Italy
	Advances in Wearable Sensor-Based Automatic Tremor Classification Patrick Locatelli and Dario Alimonti Università degli Studi di Bergamo, Italy
	Electronic systems for wearable applications: design methodologies. Daniele Comotti, Roberto Bortoletto, Matteo Pezzoli and Marco Signorelli 221e SRL. Italy
	A Telemedicine Service Platform Exploiting BT/BLE Wearable Sensors for Remote Monitoring of Chronic Patients. Massimiliano Donati, Alessio Celli, Alessio Ruiu, Sergio Saponara and Luca Fanucci University of Pisa, Italy

Monday, May 7th

15:15-16:15 **Poster Session & Coffee break**

Session Chairs: Ms. Maria Ntogramatzi and Mr. Nikolaos Karagiorgos

Twofold state assignment for FPGA-based Mealy FSMs

Alexader Barkalov, Larysa Titarenko and Kamil Mielcarek

University of Zielona Góra, Poland

Development of a Low Cost Brushless DC Motor Sensorless Controller Using dsPIC30F4011.

Y. Karnavas, A. Topalidis and M. Drakaki

Democritus University of Thrace, Greece

Acceleration of Image Classification with Caffe framework using FPGA.

D. Danopoulos, Ch. Kachris and D. Soudris

NTUA, Greece

Comparison of the R-R intervals in ECG and Oximeter signals to be used in complexity measures of Natural Time Analysis.

G. Baldoumas, D. Peschos, G. Tatsis, C. Votis, S. Chronopoulos, V. Christofilakis, P. Kostarakis, N. Sarlis, E. Skordas, K. Naka and A. Bechlioullis

University of Ioannina, Greece

Can “Memristors” be Applied in Economic Models?

O. Tacha, I. Stouboulos and I. Kyprianidis

Aristotle University of Thessaloniki, Greece

An empirical comparison of machine learning techniques for chant classification.

K. Kokkinidis, T. Mastoras, A. Tsagaris and P. Fotaris

University of Macedonia, Greece

Chaos Generator Device Based on a 32 Bit Microcontroller Embedded System

A. Giakoumis, Ch. Volos, I. Stouboulos, H. Polatoglou and I. Kyprianidis

Alexander Tech. Ed. Inst. of Thessaloniki, Greece

A new non-magnetic trimmer for the Magnetic Resonance Imaging System.

Z. Jebri, I. Bord Majek, C. Delafosse, Y. Ousten and Ch. Pasquet

IMS laboratory, Exxelia Temex, France

Monday, May 7th
Design Space Exploration of the KNN Imputation on FPGA A. Al-Zoubi, K. Tatas and C. Kyriacou Frederick University, Cyprus
Robot's Path Planning Based on Emulated Finite Resistive Grids E. Petavratzis, Ch. Volos, I. Stouboulos, I. Kyprianidis, E. Nistazakis and G. Tombras Aristotle University of Thessaloniki, Greece
Expanding a robot's life: Low power object recognition via FPGA-based DCNN deployment P. Mousouliotis, K. Panayiotou, E. Tsardoulias, L. Petrou and A. Symeonidis Aristotle University of Thessaloniki, Greece
A power management system using reconfigurable storage scheme for batteryless wireless sensor nodes. A. Siskos, F. El Mahboubi, V. Boitier, Th. Laopoulos and M. Bafleur Aristotle University of Thessaloniki, Greece
Equivalent Inverter-Based Characterization Tool for Nano-Scale CMOS Digital Cells: Non-Linear-Delay-Models Evaluation. I. Messaris, M. Ntogramatzi, N. Karagiorgos and S. Nikolaidis Aristotle University of Thessaloniki, Greece
Experimental Study of the Adaptive Body Bias on-Chip (ABBoC) for Bias Temperature Instability (BTI) and Process Variations (PV) Compensation. Hassan Mostafa American University in Cairo, Egypt
Bike Sharing as a Key Smart City Service: State of the Art and Future Developments. F. Chiariotti, C. Pielli, A. Cenedese, A. Zanella and M. Zorzi University of Padova, Italy
Design of CPLD-based Mealy FSMs with counters. A. Barkalov, L. Titarenko and S. Chmielewski Univ. of Zielona-Gora, Poland
Software Design for a Sound Processing Embedded System. G.-P. Kousiopoulos, D. Porlidas and S. Nikolaidis Aristotle University of Thessaloniki, Greece

Monday, May 7th

16:15-18:03 — **Session A3: Circuit design**

Session Chair: Prof. Alkiviadis Hatzopoulos.

A 1.2 Gbps Failsafe Low Jitter LVDS Transmitter- Receiver Applied in CMOS Image Sensor.

Wei Fan, Zhelu Li, Jianxiong Xi, Lenian He, Kexu Sun and Ning Xie

Zhejiang University, China

An RBF-PSO technique for the rapid optimization of (CMOS) analog circuits.

Amel Garbaya, Mouna Kotti, Nawel Drira, Mourad Fakhfakh, Esteban Tlelo-Cuautle and Patrick Siarry

University of Gafsa, Tunisia

Elements for Upset Hardened Associative Memories.

Yury Katunin and Vladimir Stenin

SRISA RAS, Russia

Low-Power Dual-Edge-Triggered Synchronous Latency-Insensitive Systems.

D. Konstantinou, A. Psarras, Ch. Nicopoulos and G. Dimitrakopoulos

Democritus University of Thrace, Greece

Aging Monitoring in SRAM Sense Amplifiers

Helen-Maria Dounavi, Y. Sfikas and Y. Tsiatouhas

University of Ioannina, Greece

A Very Compact Population Count Circuit for Associative Memories.

Luca Frontini, Valentino Liberali and Alberto Stabile

University of Milan, Italy

16:15-18:03 — **Session B3: Network systems**

Session Chair: Prof. Constantinos Hilas

High-Performance 3D NoC Bufferless Router with Approximate Priority Comparison.

Konstantinos Tatas

Frederick University, Cyprus

Sharing Transmission Opportunity in Ad-hoc WLANs Supporting VoIP.

Anastasios Politis and Constantinos Hilas

Tech. Ed. Inst. of Central Macedonia, Greece

Monday, May 7th	
	Novel three-level architecture for broadband fiber-optic networks. A. Boursianis, Th. Samaras and J. Sahalos Aristotle University of Thessaloniki, Greece
	Joint Task Allocation Approaches for Hierarchical Wireless Sensor Networks. Wanli Yu, Yanqiu Huang, Enjie Ding and Alberto Garcia-Ortiz University of Bremen, Germany
	SDN-based QoS Provisioning and Interference Management in Heterogeneous CRN. Ioanna Kakalou, Kostas Psannis, Katherine Siakavara, Sotirios Goudos and Yutaka Ishibashi University of Macedonia, Greece
	Design and implementation of an open-source infrastructure and an intelligent thermostat. Anastasios Loumpas, Georgios Panaras and Minas Dasygenis University of Western Macedonia, Greece

Tuesday, May 8th

08:45-09:30 — **Registration**

09:30-10:30 — **Keynote Speech 2**

Dealing with Complexity in Synthesizing System and Devices for Communication / Sensing Systems: The System-by-Design Paradigm.

Keynote Speech: Prof. Andrea Massa, IEEE Fellow, Univ. of Trento, Italy.

Chair: Prof. Sotirios Goudos.

10:30-11:00 — **Coffee Break.**

11:00-12:30 — **Session A4: Student Contest on Electronics**

Session Chair: Dr. Calliope-Louisa Sotiropoulou

FPGA Implementation of Fractional-Order Chua's Chaotic Systems.

Bahy Hassan, Ahmed Abd El-Masoud, Ayman Abd El-Kader, M. Abdelhamed, Nader Rihan, M. Tolba, Lobna Said, A. Radwan and M. Abu-Elyazeed

Cairo University, Egypt

Differentiator Based Fractional-Order High-Pass Filter Designs.

Panagiotis Bertsias and Costas Psychalinos

University of Patras, Greece.

Two Topologies of Fractional-Order Oscillators Based on CFOA and RC Networks.

Nariman Khalil, Lobna Said, A. Radwan and A. Soliman

Nahda University, Egypt

Energy-Harvesting Powered Variable Storage Topology for Battery-Free Wireless Sensors.

Firdaous El Mahboubi, Marise Bafleur, Vincent Boitier and Jean-Marie Dilhac

Laboratoire d'analyse et d'architecture des systems, France

Prototype board development for the validation of the VMM ASICs for the New Small Wheel – ATLAS upgrade project.

Panagiotis Gkountoumis

NTUA, Greece

Tuesday, May 8th

11:00-12:30	**Session B4: Student Contest on Communications** **Session Chair: Prof. Theodoros Zygiridis**
	On the Impact of Misalignment Fading in Transdermal Optical Wireless Communications. Stylianos Trevlakis, Alexandros-Apostolos Boulogeorgos and George Karagiannidis Aristotle University of Thessaloniki, Greece
	Intelligent Noncoherent Sequence equals Coherent Detection: Experimental Proof in Industrial RFID. Michail Ouroutzoglou, Aggelos Bletsas and George N. Karystinos Technical Univ. of Crete, Greece
	Development of a Transmission Line Model for the Thickness Prediction of Thin Films via the Infrared Interference Method. Ch.Mpilitos, N.Kantartzis, S.Amanatiadis, G.Apostolidis, G. Karagiannis and Th. Zygiridis Aristotle University of Thessaloniki, Greece
	Efficient Stochastic EM Studies via Dimensionality Reduction of Polynomial-Chaos Expansions. Ch. Salis, N. Kantartzis and Th. Zygiridis University of Western Macedonia, Greece
	Analysis and Design of Fully Planar CSRR-enhanced Substrate-Integrated Waveguides and Slot Antennas for 5G Communications. M. Nitas, V. Salonikios, S. Raptis and T. Yioultsis Aristotle University of Thessaloniki, Greece
12:30-13:40	**Light lunch**
13:45-15:33	**Session A5: Systems and Applications II** **Session Chair: Prof. Ahmed G. Radwan**
	Function Supervisors for Storage Systems F. Koumboulis, D. Fragkoulis and G. Diveris Tech. Educational Inst. of Sterea Ellada, Greece
	Implementation of Artificial Intelligence Based Optimally Tuned Controllers to a Class of Embedded Nonlinear System. Magdy Aboelela Cairo University, Egypt

Tuesday, May 8th	
	Trusted Hardware Sensors for Anomaly Detection in Critical Infrastructure Systems. A. Fournaris, K. Lampropoulos and O. Koufopavlou University of Patras, Greece
	Using Color Signatures for the Classification of Skin Disorders. Nikos Petrellis TEI Larissas, Greece
	Low-Cost Soft-Error Compensation for Transposed FIR Digital Filters. Vassilis Paliouras, Konstantina Karagianni, Yann Oster University of Patras, Greece
	A Tetris-based Legalization Heuristic for Standard Cell Placement with Obstacles. P. Oikonomou, A. Dadaliaris, T. Loukopoulos, A.Kakarountas and G. Stamoulis. University of Thessaly, Greece
13:45-15:33	**Session B5: Antennas and propagation** **Session Chair: Prof. Stavros Koulouridis**
	Printed Antennas with Enhanced Performance for Rectenna Applications. Apostolia Karampatea and Katherine Siakavara Aristotle University of Thessaloniki, Greece
	Design of Ultra-Wide Band Slot Antennas for Future 5G Mobile Communication Applications. Ioannis Gerafentis and Katherine Siakavara Aristotle University of Thessaloniki, Greece
	Outage Performance of Mixed, Parallel and Serial, DF Relayed FSO Links over Weak Turbulence Channles with Nonzero Boresight Pointing Errors. G. Varotsos, H.E. Nistazakis, A. Stassinakis, G. Tombras, V. Christofilakis and Ch. Volos UOA, Greece
	Rainfall events' correlation with S-band signal attenuation. G. Tatsis, C. Votis, V. Christofilakis, S. Chronopoulos, P. Kostarakis, Ch. Lolis, A. Bartzokas and H. Nistazakis University of Ioannina, Greece

Tuesday, May 8th	
	Characteristic Mode Analysis of Drop-like Supershaped Patch Antenna. K. Samaras, R. Maximidis, A. Koutinos, G. Ioannopoulos, D. Caratelli, J. Sahalos and G. Kyracou Democritus University of Thrace, Greece
	Bandwidth Enhancement of Rectangular Patch Antennas Using Multiple Feeding Points: A Review. A. Koutinos, G. Ioannopoulos, M. Chryssomallis and G. Kyriacou Democritus University of Thrace, Greece
15:33-16:30	**Poster Session & Coffee Break** **Session Chair: Dr. Achilles Boursianis**
	Spiral Inductor Design Based on Fireworks Optimization Combined with Free Search. Daniel Cavalcanti Jeronymo, Jean Vianei Leite, Viviana Cocco Mariani, Leandro Dos Santos Coelho and Sotirios Goudos Federal University of Technology – Parana, Brazil
	Multiobjective Lightining Search Applied to Jiles-Atherton Hysteresis Model Parameter Estimation Leandro Coelho, Juliano Pierezan, Nelson Jhoe Batistela, Jean Vianei Leite and Sotirios Goudos Pontifícia Universidade Católica do Parana, Brazil
	Information Security Awareness of Greek Higher Education Students - Preliminary Findings. Adam Filippidis, Constantinos Hilas, Georgios Filippidis and Anastasios Politis Stockholm University, Sweden
	An Ultra-Low-Power RF Receiver for IoT Applications using 65nm CMOS Technology. Sameh Abdelbadie, Andrew Mikhael, Mostafa Helmy, Bassel Elgharabawy and Ahmed Mohieldin Cairo University, Egypt
	Power Saving Issues in a Low Cost eHealth Sensor Controller. N. Petrellis, M. Birbas, M. Vardakas and I.E. Kosmadakis TEI Larissas, Greece

Tuesday, May 8th	
	Mathematical Analysis of Gene Regulation Activator Model Samar Ismail, Lobna Said, Ahmed Madian, Ahmed Radwan and Mohamed Abu-Elyazeed GUC University, Egypt
	Efficiency Comparison of Charge Pump DC/DC Configurations for Energy Harvesting. Roberto Rafael Flores Quintero and Guillermo Espinosa Flores-Verdad National Institute of Astrophysics Optics and Electronics, Mexico
	An Enhanced Simulation Model for DC Motor Belt Drive Conveyor System Control. A. Katsioula, Y. Karnavas and Y. Boutalis Democritus University of Thrace, Greece
	A Low Power, Offset Compensated, CMOS Only Bandgap Reference in 22 nm FD-SOI Technology. Prajith Kumar Poongodan, Pragoti Pran Bora, Borggreve David, Frank Vanselow and Linus Maurer Fraunhofer EMFT Research Institution for Microsystems and Solid State Technologies, Germany
	Efficiency Evaluation of a SystemVerilog-based Real Number Model. Nikolaos Georgoulopoulos and Alkiviadis Hatzopoulos Aristotle University of Thessaloniki, Greece
	Dynamically Reconfigurable Power Efficient Security for Internet of Things Devices. Khaled Khateb, Mostafa Ahmed, Ahmed Kamal Eldin, Mohamed Abdelghany and Hassan Mostafa German University in Cairo, Egypt
	Overview Study of On-chip Interconnect Modelling Approaches and Its Trend. Mohammed Al-Daloo, Ahmed Soltan and Alex Yakovlev Newcaste Univ. UK.
	Time-Based Read Circuit for Multi-Bit Memristor Memories H. Hossam, M. Dessouki and H. Mostafa Cairo University, Egypt
	CDMA Radio on FSO Links over Gamma Turbulence Channels with Nonzero Boresight Pointing Errors M. Ninos, H.E. Nistazakis, A. Stassinakis, G. Tombras, V. Christofilakis and A. Tsigopoulos University of Athens, Greece

Tuesday, May 8th	
	Estimation of the influence of Vanadium Dioxide Optical Filters at the Performance of Visible Light Communication Systems. D. Manousou, A. Stassinakis, E. Syskakis, H.E. Nistazakis, G. Tombras, Ch. Volos and A. Tsigopoulos. National and Kapodistrian Univ. of Athens, Greece
	Extending a 65 nm CMOS Process Design Kit for High Total Ionizing Dose Effects. A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H.D. Koch, K. Kloukinas, T.S. Poikela and F. Faccio. Technical University of Crete, Greece
	A Survey on Spectrum Sensing Algorithms for Cognitive Radio Networks. I. Kakalou, D. Papadopoulou, Th. Xifilidis, K. Siakavara, Y. Ishibashi and K. Psannis. University of Macedonia, Greece
	A novel algorithm and hardware architecture for low-complexity soft demappers. Andreas Kalampoukas and Vassilis Paliouras University of Patras, Greece
	Prototype wireless sensor network for real-time measurements in hydroponics cultivation. A. Theopoulos, A. Boursianis, A. Koukounaras and Th. Samaras Aristotle University of Thessaloniki, Greece
16:30-18:30	**Tutorial** **Converged Optical-Wireless Networks: an Effective Solution for 5G Network Architectures.** **Speakers: Dr. John Vardakas, Iquadrat Informatica S.L., Spain and Dr. Christos Verikoukis, Telecommunications Technological Centre of Catalonia, Spain.**
21:00-	**Social Dinner (If Registered)**

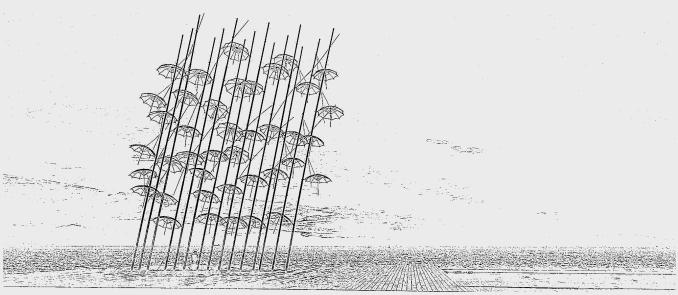
Wednesday, May 9th

09:20-10:00	**Registration**
10:00-10:30	**Invited Speech 1:** **Connecting the Dots: A Big Data Paradigm!** **Speaker: Dr. Calliope-Louisa Sotiropoulou, INFN Pisa, Italy** **Chair: Prof. Kostas Siozios**
10:30-11:00	**Invited Speech 2:** **Fiber as key enabler for 5G deployments.** **Speaker: Mr. Thanos Mantzoros, Victus Manager, Athens** **Chair: Prof. Sotirios Goudos**
11:00-11:30	**Coffee Break**
11:30-13:00	**Session A6: Memristors and chaos-based behavior** **Session Chair: Dr. Stavros Stavrinides.**

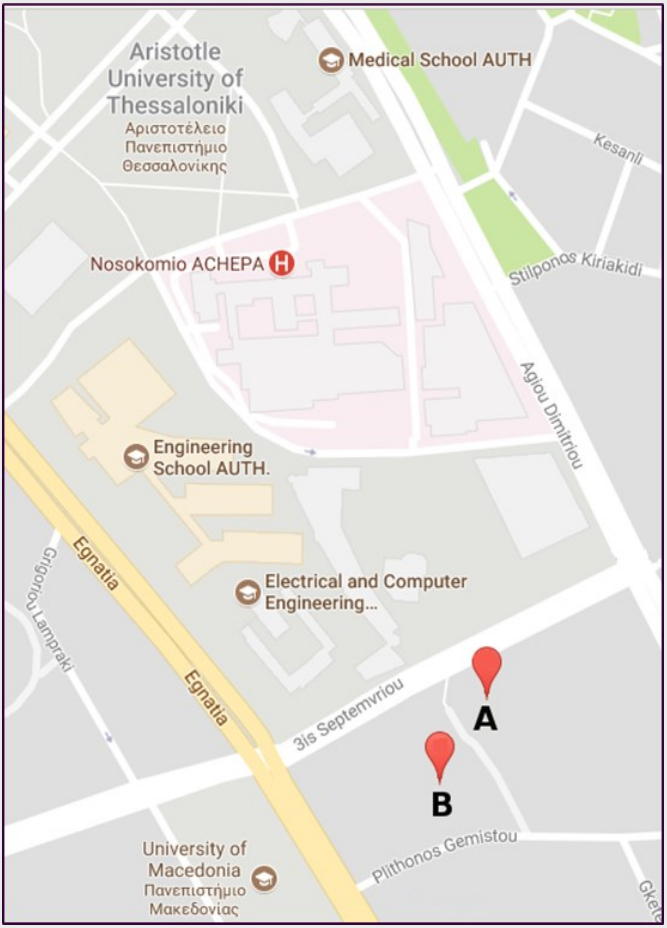
Emulating Memristors in a Digital Environment using Stochastic Logic. O. Camps, R. Picos, C. de Benito, M. Moner Al Chawa and S. Stavrinides Universitat de les Illes Balears, Spain
Study of Fractional Flux-controlled Memristor Emulator Connections. Abdulaziz Elsafty, Esraa Hamed, Ahmed Madian, Ahmed Radwan, Lobna Said and Mohamed Fouda Nile University, Egypt
Integrator Device with a Memristor Element Stoyan Kirilov and Valeri Mladenov Technical University of Sofia, Bulgaria
Experimental Measurements on Resistive Switching Devices: Gaining Hands-on Experience. J. Gomez, I. Vourkas, A. Abusleme and G. Ch. Sirakoulis Pontificia Universidad Catolica de Chile, Chile
Chaos-Based Hardware Speech Encryption Scheme Using Modified Tent Map and Bit Permutation. Mohammed Tolba, Wafaa Saber, Ahmed Radwan and Salwa Abd-El-Hafiz Nile University, Egypt

Wednesday, May 9th

11:30-13:00	**Session B6: High performance embedded systems** **Session Chair: Prof. Kostas Siozios**
	Streaming Data Correlation on GPUs. S. Fotopoulos, P. Malakonakis, G. Chrysos and A.Dollas Technical University of Crete, Greece
	Efficient Support Vector Machines Implementation on Intel/ Movidius Myriad 2. Ch. Marantos, N. Karavalakis, V. Leon, V. Tsoutsouras, K. Pekmestzi and D. Soudris National Technical University of Athens, Greece
	Design and implementation of a re-configurable embedded system for capacitive sensor array interface. I. Zafeirakis, M.K. Filippidou, S. Chatzandroulis, E. Kyriakis - Bitzaros, N. Stathopoulos and S. Vassiliadis NCSR "Demokritos", Greece
	Development of the Address in Real Time (ART) Data Driver Card (ADDC) test procedures of the New Small Wheel Upgrade Project. D. Matakias, Lin Yao, G. Iakovidis and Th. Alexopoulos National Technical Univ. of Athens, Greece.
	Logarithmic Number System for Deep Learning. Ioannis Kouretas and Vassilis Paliouras University of Patras, Greece
13:00-13:30	**Awards - Closing ceremony**



Useful Information



A: Conference Venue: Aristotle University Research Dissemination Center (ΚΕΔΕΑ – ΚΕΔΕΑ).
3is Septemvriou str, Aristotle University Campus, Thessaloniki

B:Lunch Venue: Café Roof Garden (Next to the Conference Venue).

Access to the Wireless Internet: Please ask at the Registration Desk, in order to provide to you a password and login details.

The Certificates of Attendance will be available from Tuesday, May 8th afternoon. Please, do not forget to collect your certificate from the Registration Desk.

The Conference Dinner will be offered at the restaurant Dore Zythos "ΝΤΟΡΕ ΖΥΘΟΣ" at the area of White Tower. (address: Tsirogianni 7 str/ Τσιρογιάννη 7). Advanced registration is required.

At a glance

Monday, May 7th

08:30-09:00	Registration
09:00-09:30	Opening
09:30-10:30	Keynote Speech 1: Prof. Dietmar Fey
10:30-11:00	Coffee Break
11:00-12:30	Session A1: Systems and Applications I
	Session B1: Communication systems
12:30-13:40	Light Lunch
13:45-15:15	Session A2: Modeling, Simulation and Power Management
	Session B2: Special Session on Wearable Sensor Systems
15:15-16:15	Poster Session - Coffee Break
16:15-18:03	Session A3: Circuit design
	Session B3: Network systems

Tuesday, May 8th

08:45-09:30	Registration
09:30-10:30	Keynote Speech 2: Prof. Andrea Massa
10:30-11:00	Coffee Break
11:00-12:30	Student Session A4: Electronics
	Student Session B4: Communications
12:30-13:40	Light Lunch
13:45-15:33	Session A5: Systems and Applications II
	Session B5: Antennas and Propagation
15:33-16:30	Poster Session - Coffee Break
16:30-18:30	Tutorial: Dr. John Vardakas, and Dr. Christos Verikoukis.
21:00 -	Dinner

Wednesday, May 9th

09:20-10:00	Registration
10:00-10:30	Invited Speech 1: Dr. Calliope-Louisa Sotiropoulou
10:30-11:00	Invited Speech 2: Mr. Thanos Mantzoros
11:00-11:30	Coffee Break
11:30-13:00	Session A6: Memristors and chaos-based behavior
	Session B6: High performance embedded systems
13:00-13:30	Awards - Closing ceremony