

FTK Input Mezzanine and Data Formatter for the Fast Tracker at ATLAS

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Abstract—The Fast Tracker (FTK) is an integral part of trigger upgrade program for the ATLAS detector. LHC restarts operations in March 2015 at a center of mass energy of 13 TeV and an average of 40-50 simultaneous proton collisions per beam crossing. The higher luminosity demands a more sophisticated trigger system with increased use of tracking information. However, the combinatorial problem posed by charged particle tracking becomes increasingly difficult due to the large number of multiple interactions per bunch crossing.

The FTK is a highly-parallel hardware system that rapidly reconstructs tracks in the ATLAS inner-detector for every event that passes the Level-1 trigger at a maximum event rate of 100 kHz. This paper focuses on the FTK Input Mezzanine card (FTK_IM) and Data Formatter (DF) boards that are the input interface and the first processing stage of the FTK system. The board design, combined test results, and production status are reported.

I. INTRODUCTION

AFTER a very successful data taking run, the ATLAS experiment [1] is being upgraded to cope with the higher luminosity and higher center-of-mass energy that the Large Hadron Collider (LHC) will provide in the next years. The higher instantaneous luminosity expected at the LHC Run 2 will pose challenges for the trigger system. The existing ATLAS trigger system, consisting of a hardware-based Level-1 trigger and a CPU-based High Level Trigger (HLT), was designed to work well at the LHC design luminosity, $10^{34} \text{cm}^{-2} \text{s}^{-1}$. However after the planned luminosity upgrade, the detector environment will be complicated by the increase in detector activity arising from many simultaneous interactions. Because of its fine resolution, tracking information is critical for distinguishing which events triggered by the Level-1 should be kept for further processing.

An electronics system, the Fast Tracker (FTK) [2], is part of ATLAS strategy to cope with this environment. It will do global track reconstruction after each Level-1 trigger to enable the HLT to have early access to tracking information. Figure 1 shows the functional overview of the FTK system. FTK will use data from the pixel (PIX) and semiconductor

tracker (SCT) detectors as well as the new Insertable B-Layer (IBL) of pixel detector [3]. FTK will move track reconstruction into a hardware system with massively parallel processing that produces global track reconstruction with good resolution just after the start of HLT processing.

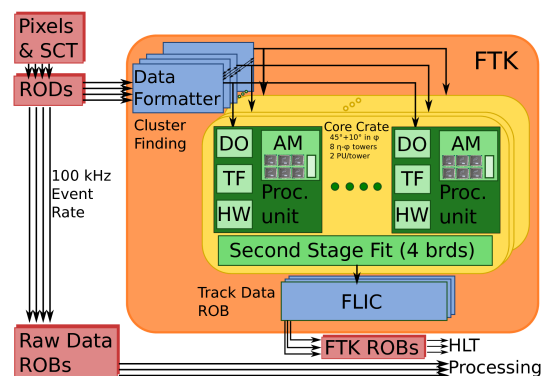


Fig. 1. Functional overview of the FTK hardware system

This paper focuses on the FTK Input Mezzanine cards (FTK_IM) and Data Formatter (DF) boards [4] which are the input interface and the first processing stage of the FTK system.

II. HARDWARE DESCRIPTION

To deal with the large input rate as well as the large number of hit combinatorics at high luminosity, FTK is highly parallel. The system is segmented into 64 $\eta - \phi$ towers, each with two processing units. FTK uses 12 logical detector layers (4 pixel including IBL and 8 SCT layers) over the full rapidity range covered by the barrel and the disks. The FTK_IM and DF are the input interface of FTK system which receives inner detector data and distributes it to downstream system. Functional details and components of FTK_IM and DF are described.

A. FTK Input Mezzanine

The functions of the FTK_IM are to receive the PIX and SCT data from the ATLAS Silicon Read-Out Drivers (RODs), perform clustering, and then forward the data to the DF. The FTK_IM functions are implemented in a mezzanine card that connects to DF motherboard with a high pin count version of an FMC connector. Each FTK_IM receives up to 4 S-LINK optical fibers from RODs through four SFP+ connectors. On the mezzanine there are 2 FPGAs. Each FPGA receives two links, one from PIX and the other from SCT SLink, processes data independently, and transmits the output to the FMC connector. In each FPGA, clustering is performed for both pixel and micro-strip data in order to reduce the amount of data to be processed by downstream FTK electronics. It additionally determines the cluster center for improved spatial resolution. For the data transfer from FTK_IM to DF, Double Data Rate (DDR) source-synchronous parallel bus of LVDS operated at 200MHz is used. The Inter-Integrated Circuit (I2C) bus is used for slow control of FTK_IM from DF.

B. Data Formatter

As noted previously, FTK is organized as a set of parallel processor units within an array of $64 \eta - \phi$ towers. To avoid inefficiency at tower boundaries, the towers must overlap because of the finite size of the beam's luminous region in z and the finite curvature of charged particles in the magnetic field.

The DF board receives the hits from the FTK_IM, remaps the ATLAS Inner Detector geometry to match the FTK $\eta - \phi$ tower structure, performs data switching in overlap regions, and delivers the hits to the Processor Units. 32 DF boards will be used to handle 64 FTK $\eta - \phi$ towers. For the design requirements, a system based on an Advanced Telecommunications Computing Architecture (ATCA) technology with the full-mesh backplane interconnect is found to be a natural solution for the DF design. All DF boards in one ATCA shelf are directly connected using multiple point-to-point high-speed serial links over the backplane for the data formatting. A Virtex-7 FPGA on each DF board is the main processing engine. The dedicated input data are efficiently remapped and shared among the DF boards over the full-mesh backplane and dedicated inter-shelf fiber links to minimize the system latency. The Rear Transition Module (RTM) is used to send the data to downstream of FTK as well as to perform inter-crate data switching. The output data will be sent to over 288 QSFP fiber links to the tracking core units. Figure 2 shows the DF implemented with 4 IMs.

III. HARDWARE TEST AND PRODUCTION STATUS

Each functionality of the boards must be fully tested and bit error rates (BER) for all the lines must satisfy the ATLAS requirement ($BER < 10^{-15}$) before mass production to validate that FTK works at the design spec under the high luminosity environment. A full chain integration test is being performed at CERN. The goal of the test is to achieve stable dataflow with full FTK functionality with 100kHz level-1 trigger event rate throughout full FTK chain.

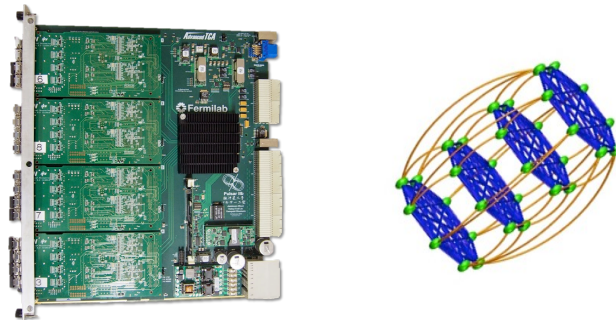


Fig. 2. The Data Formatter board with 4 FTK Input Mezzanines (left). A graphical depiction of the 32 boards (in green) and high speed interconnect lines in four crate system. Blue lines represent backplane data paths. Orange lines represent inter-crate fiber links (right).

A. Status of the FTK_IM

Prototype FTK_IM boards identical to the production version are ready and being tested. It is confirmed that FTK_IM is linked-up with Inner Detector RODs and receives hit data. The clustering firmware is implemented for both SCT and Pixel. The DDR data transfer between Data Formatter is running at design level of 200MHz. With 4 FTK_IMs mounted on 1 DF board, stable dataflow is achieved at 100kHz event rate using full 16 input channels, with the clustering functionality working. For configuration and monitoring, I2C bus is fully tested and in use. Several monitoring registers are defined and read out via I2C bus. They will be added as necessary. Bit error rate of all the lines are measured and confirmed to satisfy ATLAS requirement. The validation of the output data is ongoing, by comparing it with the output of software simulation. And other detailed improvements are ongoing.

80 FTK_IMs are mass produced. A quick check was done and the mass production found to be in good shape. Quality control tests were performed in March 2015. All lines and components of all the 80 FTK_IMs were checked in detail. After completing quality control test, they will be ready to install and delivered to CERN.

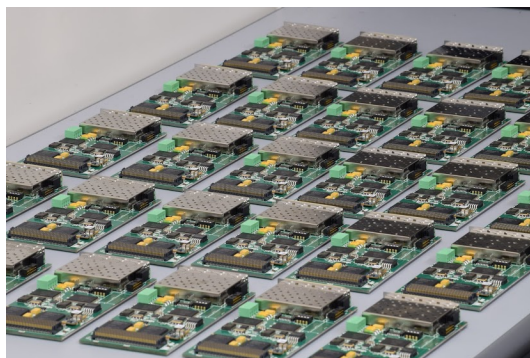


Fig. 3. Mass production of 80 FTK_IMs are done. Quality control test will be performed, and they will be delivered to CERN after completing the quality control test.

B. Status of the Data Formatter

Prototype boards are ready and being tested in ATCA shelf in CERN test lab. Tests for 8 boards in a crate is ongoing at FNAL. Initial switching firmware is ready and being tested. It is confirmed that DF receives clustered data from FTK_IM and forward it to the downstream with full 16 input channels at 100kHz input rate. Bit error rate of all the input, output and inter-connection lines are measured and confirmed to satisfy ATLAS requirement. The RTM board is also tested and $BER < 10^{-15}$. The interface for the next downstream board is established at the required speed. For user interface of monitoring and configuration, a star network of 1000 Base-T Ethernet are in use and tested over ATCA backplane fabric interface for IPbus.

The mass production of DF is started and phased production is performed. The boards will be received and installed at CERN over the summer.

IV. CONCLUSION

FTK provides full detector track information for events accepted by Level-1 trigger, which allows more processing capacity for HLT. FTK_IM and DF boards are the input interface and the first processing stage of the FTK system. Prototype boards for both FTK_IM and DF board are ready and being tested. Mass production of FTK_IM and DF are ongoing. After completing the integration test and the mass production, FTK will be installed for the barrel region ($|\eta| < 1.0$) at late 2015, and full coverage ($|\eta| < 2.5$) will be established in 2016.

REFERENCES

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