Level-1 Data Driver Card of the ATLAS New Small Wheel upgrade

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***Abstract*—The Level-1 Data Driver Card (L1DDC) will be fabricated for the needs of the future upgrades of the ATLAS experiment at CERN. The L1DDC board is a high speed aggregator board capable of communicating with a large number of front-end electronics. It collects the Level-1 along with monitoring data and transmits them to a network interface through a single bidirectional fibre link. Finally, the L1DDC board distributes trigger, time and configuration data coming from a network interface to the front-end boards.**

This paper describes the overall scheme of the data acquisition process and especially the L1DDC board for the upgrade of the New Small Wheel. Finally, the electronics layout on the chamber is also mentioned.

I. Introduction

The future upgrades of the LHC will lead to an average luminosity of $5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$. The number of interactions will be increased at about 140 interactions per bunch crossing ($25\,\mathrm{ns}$) resulting in a dramatically large amount of produced data. In the ATLAS experiment [1] the present muon Small Wheels will be replaced by the New Small Wheels (NSW). The NSW is a set of precision tracking and trigger detectors able to work at high rates with excellent real-time spatial and time resolution. The new detectors consist of the resistive micromegas and the small Strip Thin Gap Chambers (sTGC) [2].

Furthermore, a radiation dose of about $1700\,\mathrm{Gy}$ (inner radius) and a magnetic field $< 0.4\,\mathrm{T}$ at the end cap region, create a hostile environment for the electronic components. To readout the high number of electronics channels and in order to survive in such a harsh environment new electronics must be fabricated. In addition, Single Event Upset (SEU) mechanisms must be implemented to assure the integrity of the transmitting data.

The L1DDC is an intermediate board that aggregates and transmits the Level-1 data (time, charge and strip address corresponding to a single hit) from multiple front-end boards to a network called Front End LInk eXchange (FELIX). This is achieved using a high speed serializer/deserializer ASIC called GigaBit Transceiver (GBTX) developed at CERN. In general, the L1DDC combines three distinct paths: Timing, Trigger and Control (TTC) [3] data, Data Acquisition and Slow Control information, into one bidirectional optical link at a rate of 4.8 Gbps, as shown in Figure 2.

II. Connectivity

Front-end boards [5] include three ASICs, the VMM [6], the Read Out Controller (ROC) and the Slow Control Adapter (SCA). The VMM provides trigger and tracking primitives for 64 channels. The ROC ASIC collects the Level-1 data from the VMMs and transmits them to the L1DDC through a serial stream. Also, the ROC ASIC receives the TTC and the Level-1 accept data from the FELIX. Finally, the SCA ASIC is responsible for configuring the VMMs receiving the configuration data from the L1DDC and for transmitting the monitoring data through the L1DDC to the FELIX, as shown in Figure 1.

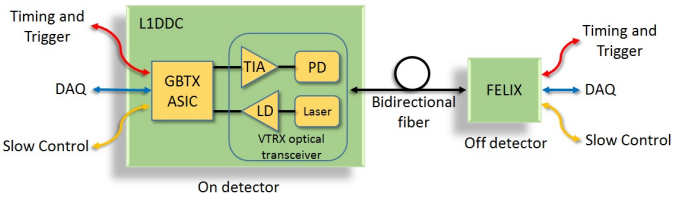


Fig. 2: On the left side the L1DDC, which resides on the detector and is implemented with custom ASICs, combines the three district paths (Timing and Trigger, DAQ, Slow Control) into a single bidirectional optical link.

The GBTX ASIC is capable of multiplexing a number of serial links (e-links) to a single fibre. One e-link, consists of three differential pairs (6 wires) being the clock (Clk+ and Clk-), the data in (Din+ and Din-) and the data out (Dout+ and Dout-), as shown in Figure 3. The GBTX ASIC can support up to 40 e-links divided in five groups called banks. Each bank can support up to eight e-links at $80\,\mathrm{Mbps}$, four e-links at $160\,\mathrm{Mbps}$ or two e-links at $320\,\mathrm{Mbps}$.

For the micromegas detectors the L1DDC is connected to the front-end board through a single twinax cable that carries two e-links. The one e-link is connected to the ROC ASIC and the other e-link to the SCA ASIC, as shown in Figure 1. In total, eight front-end boards will be connected to one L1DDC board contrary to the sTGC detectors where only three front-end boards will be connected to one L1DDC board. The

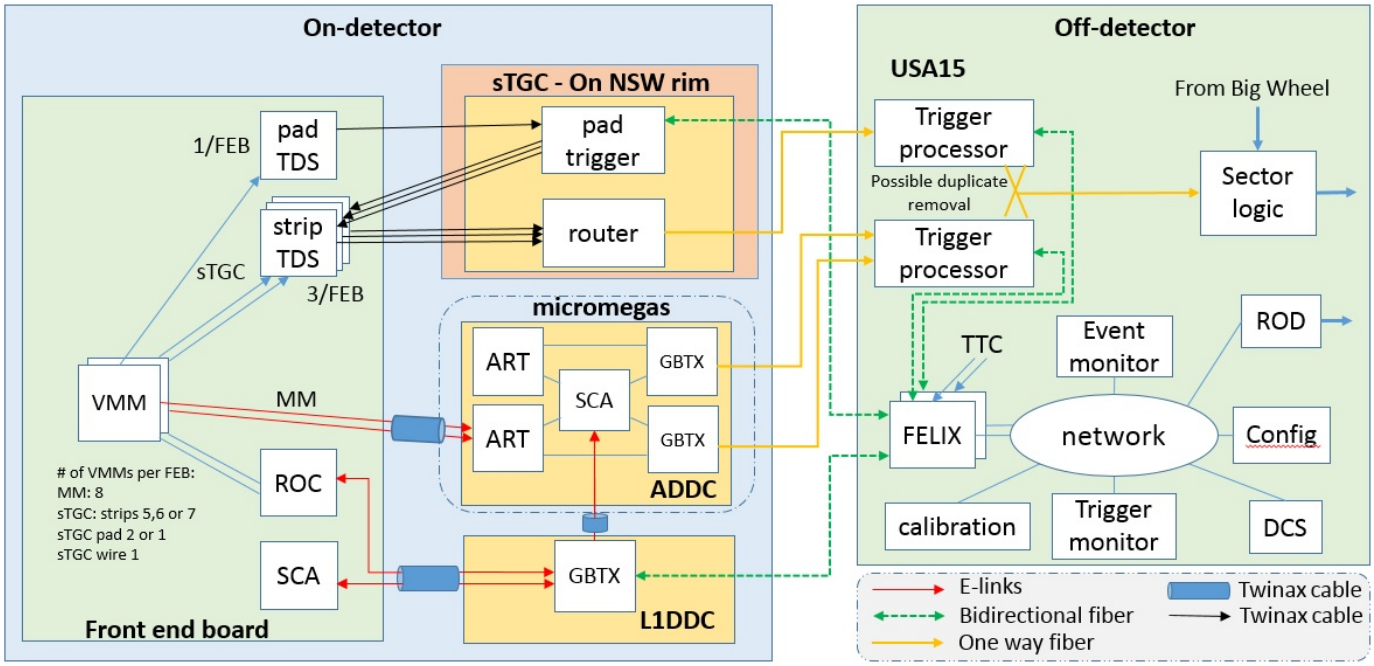


Fig. 1: NSW electronics trigger and dataflow. L1DDC is connected to the ROC and the SCA ASIC of the front-end boards with one e-link each. One e-link and two extra differential pairs are used for the connection to the ADDC boards and a bidirectional optical link is used for the communication to the FELIX.

connection will also be through twinax cables but in this case ten differential pairs are used in each cable.

Data rate simulations showed that for the inner portions of the micromegas detector the bit rate will exceed 320 Mbps. For this reason, for the inner two front-end boards, a special configuration scheme will be implemented. One e-link with 320 Mbps and one e-link with 160 Mbps is connected to the inner two front-end boards, resulting in a sum of 480 Mbps each. The next four front-end boards have a bit rate of 320 Mbps and finally the outer 2 front-end boards, have a bit rate of 160 Mbps.

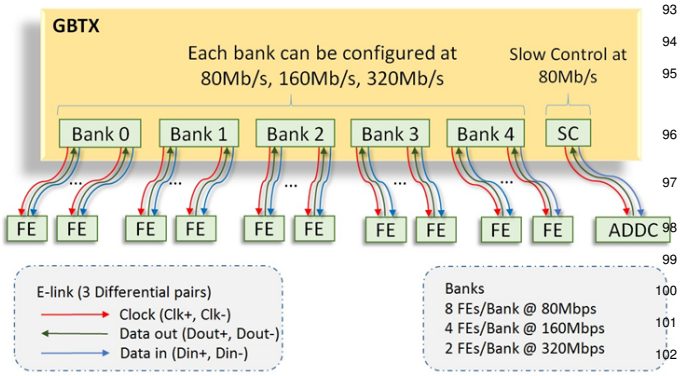


Fig. 3: GBTX e-link connectivity. There are five banks which support up to 40 FE boards. In each bank eight FE boards can be connected at 80 Mbps, four at 160 Mbps or two at 320 Mbps. An extra Slow Control e-link with a fixed rate at 80 Mbps is used for the connection to the ADDC board.

With this configuration the fifth spare bank of the GBTX is used for the communication with the SCA ASICs of each MMFE at the 80 Mbps data rate. The GBTX ASIC has an extra Slow Control (SC) e-link with a fixed rate at 80 Mbps for slow control information. This extra e-link will be used for the connection to the ADDC (Address in real time Data Driver Card) [4] boards. The ART signals of the eight MMFE boards are multiplexed into the ADDC board.

The L1DDC provides configuration data, clocks and the Bunch Crossing Reset (BCR) signal to the ADDC board. The communication between the ADDC and L1DDC is done through one e-link for the configuration data and four extra differential pairs for the clocks and the BCR signals. As mentioned above, the L1DDC will communicate with the FELIX through a bidirectional optical link.

III. Functionality

A. GBTX functionality

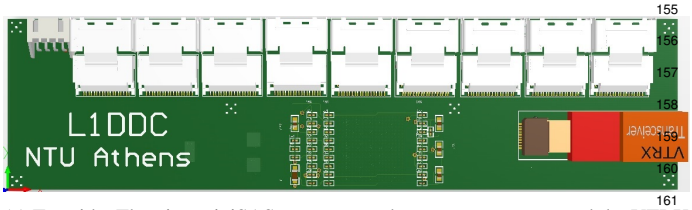
The GBTX is a full radiation tolerant ASIC fabricated using the 130 nm technology. Its power supply is 1.5 V and its power consumption is 2.2 W in full operation. E-links use Scalable Low-Voltage Signalling (SLVS) for 400 mV (SLVS-400) [8]. The SLVS is a differential standard with a swing of 200 mV, centred on 0.2 V. The transmitting data use the Double Data Rate (DDR) signalling. The GBTX ASIC has a Clock and Data Recovery (CDR) circuit which receives high speed serial data from the GBTIA. It recovers and generates an appropriate high speed clock to correctly sample the incoming data stream. The serial data is then de-serialized

and then DECoded, with appropriate error corrections, and finally DeSCRambled (DSCR). In the transmitter part the data are SCRambled (SCR), to obtain DC balance, and then encoded with a Forward Error Correction (FEC) code before being serialized and sent to the GBLD laser driver [7].

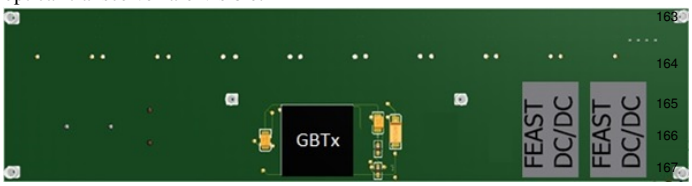
The GBTX ASIC has registers for permanent storage that are called e-fuses. Initial configuration information is taken from the e-Fuses, which can then be modified via the optical link itself or via an I^2C slave interface. Finally, GBTX has a JTAG interface for boundary scan [7].

B. L1DDC board description

Because of the different characteristics of both detector technologies, different boards will be fabricated for micromegas and sTGC detectors. Both boards will use the same components, with the difference that in micromegas detectors eight front-end boards will be connected to one L1DDC, contrary to the sTGC detectors where only three front-end boards will be connected to one L1DDC. The size of the L1DDC board for the micromegas detectors will be $200\,\mathrm{mm}$ in length, $50\,\mathrm{mm}$ in width and $18\,\mathrm{mm}$ in height as shown in Figure 4. Contrary, the size of the L1DDC for the sTGC detectors will be $90\,\mathrm{mm}$ in length, $50\,\mathrm{mm}$ in width and $18\,\mathrm{mm}$ as shown in Figure 5.



(a) Top side. The nine miniSAS connectors, the power connector and the VTRX optical transceiver are visible.

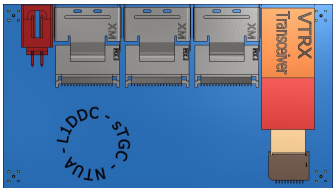


(b) Bottom side. The GBTX ASIC, the DC-DC converters and the position pins are visible.

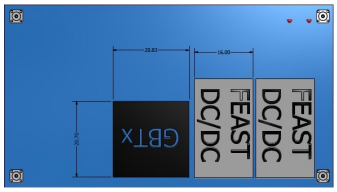
Fig. 4: A trivial 3D representation of the L1DDC board for the micromegas detectors

The communication between the ADDC, MMFE8 and L1DDC boards is made through twinax cables and mini Serial Attached SCSI (SAS) connectors. These high routable cables can support up to 12 differential pairs and the small size of the 36 position connectors makes them suitable for the boards.

Except of the GBTX ASIC, L1DDC will contain three more radiation tolerant ASICs: the GigaBit TransImpedance Amplifier (GBTIA), the GigaBit Laser Diode (GBLD) and the FEAST DC-DC converter [12]. The GBTIA and the GBLD ASICs compose the Versatile optical Transceiver (VTRX). The GTIA [9] has a bit rate of $5\,\mathrm{Gb/s}$ (min) and a total jitter smaller than $40\,\mathrm{ps}$. Its supply voltage is $2.5\,\mathrm{V}$ and its power consumption is $250\,\mathrm{mW}$ [10]. The GBLD is also a radiation tolerant ASIC fabricated in $130\,\mathrm{nm}$. It has also a bit rate of $5\,\mathrm{Gb/s}$ (minimum), supply voltage of $2.5\,\mathrm{V}$ and its power consumption is about $325\,\mathrm{mW}$ [11]. The VTRx is the largest component on the L1DDC board with a width of $45.3\,\mathrm{mm}$, a length of $14.5\,\mathrm{mm}$ and a height of $10\,\mathrm{mm}$. Figure 4 shows a preliminary 3D representation of the L1DDC board.



(a) Top side. The 3 miniSAS connectors, the power connector and the VTRX transceiver are visible.



(b) Bottom side. The GBTX ASIC, the DC-DC converters and the position pins are visible.

Fig. 5: A trivial 3D representation of the L1DDC for the sTGC detectors

The overall power consumption of the L1DDC is estimated to be $3.5\,\mathrm{W}$. In order to step down the voltage to the appropriate levels, the FEAST DC-DC converter is used. This converter has an input voltage range from $5\,\mathrm{V}$ to $12\,\mathrm{V}$, $4\,\mathrm{A}$ load capacity and achieves a $76\,\%$ efficiency. It contains a radiation tolerant ASIC with total ionizing dose up to $200\,\mathrm{Mrad}$ (Si) and displacement damage up to $5 \times 10^{14}\,\mathrm{n/cm^2}$. The FEAST has been designed for operation in a strong magnetic field in excess of $40,000\,\mathrm{Gauss}$ ($4\,\mathrm{T}$), and has been optimized for air-core inductors of $400 - 500\,\mathrm{nH}$. To power the L1DDC board with the two appropriate voltage levels ($2.5\,\mathrm{V}$ and $1.5\,\mathrm{V}$), two FEAST devices are used. The $1.5\,\mathrm{V}$ analog voltage for the GBTX PLLs is provided from the same FEAST device after filtering.

C. Frame format

The GBTX transmits frames of $120\,\mathrm{bits}$ in the interval of $25\,\mathrm{ns}$ (BC clock), resulting in a line rate of $4.8\,\mathrm{Gbps}$. Four bits are used for the frame header (H) and 32 are used for Forward Error Correction (FEC). So, the data transmission is limited to 84 bits, corresponding to a user bandwidth of $3.36\,\mathrm{Gbps}$. From the 84 bits, the four are dedicated for Slow Control (SC) information (Internal Control (IC) and External Control (EC) fields) as outlined in Figure 6.

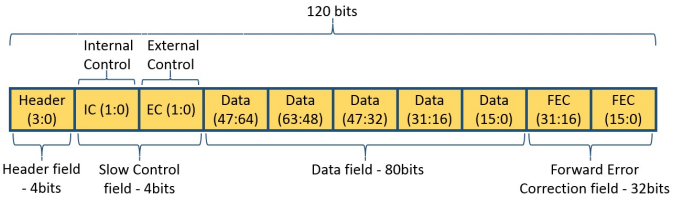


Fig. 6: GBTX frame format

The FEC algorithm is built by interleaving two Reed-Solomon RS(15,11) encoded words with 4-bit symbols, each capable of correcting a double symbol error. This means that a sequence of up to 16 consecutive corrupted bits can be corrected. Finally, all configuration registers inside the GBTX

ASIC are fully protected against SEUs with triple redundant registers [7].

IV. On detector placement

For the micromegas detectors, each L1DDC board is connected to eight front-end and one ADDC boards. The location of the L1DDC on the micromegas detectors will be radially along both sides of the wedge as shown in Figure 7. This provides a way of equalizing the load on both sides of the detector and the cable routing.

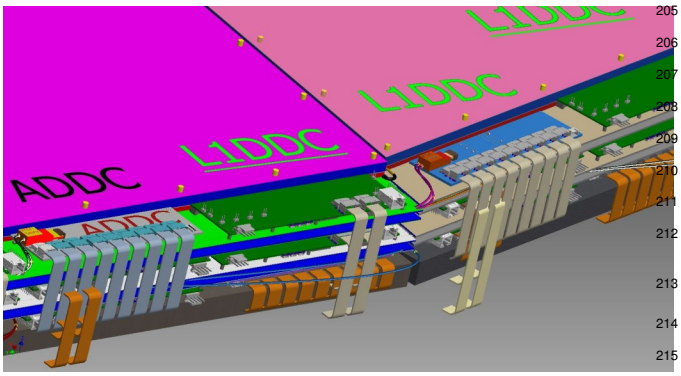


Fig. 7: MMFE, ADDC and L1DDC placement on a micromegas wedge.

In the case of micromegas detectors, a single L1DDC serves the eight front-end boards for the one side of the plane. There are 16 front-end boards in every plane resulting in 64 per wedge. This means that eight L1DDC boards are needed for every wedge. Also, there are two wedges in every sector and there are 16 sectors in every wheel. Summarizing, 512 L1DDC are needed in the micromegas detectors and 512 for the sTGC detectors resulting in a total 1024 of L1DDC boards [2].

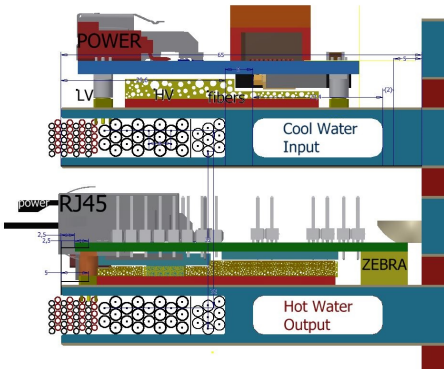


Fig. 8: In the upper part of the picture, the L1DDC board placed on a micromegas detector is illustrated. On the top side of the board the mini SAS connector, the power connector and the VTRX are placed and on the bottom side the GBTX and the DC-DC converters are placed. These components are attached to the cooling channel with the help of an elastic thermal foam. Finally, on the bottom side of the picture the FE board is also visible.

All the connectors will be placed on the top side of the board and the components that dissipate heat on the bottom side. These components with the help of a elastic thermal foam will be attached to a cooling channel in order to keep the heat at a low level.

V. Conclusion

The L1DDC board is the intermediate board responsible to collect the Level-1 data and to distribute the TTC and Level-1 accept data to the front-end electronics. It is capable to handle a large amount of data and is fully compliant with the HL-LHC rates. In addition, L1DDC is a radiation tolerant board equipped with SEU mechanisms in order to assure the signal integrity. Its dimensions are relatively small in order to fit between two readout panels of the micromegas chambers of the NSW detector for the upgrade of the ATLAS experiment. Finally, the L1DDC board must have a high reliability as after the installation of the NSW it will not be accessible for replacement.

Acknowledgments

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