Hot carrier degradation modeling of short-channel n-FinFETs suitable for circuit applications

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***Abstract*— The hot-carrier (HC) degradation of short-channel n-FinFETs is investigated. The experiments indicate that the interface degradation is accompanied with charge injection into the gate dielectric defects over the entire channel length. The relation of the hot-carrier degradation with stress time, channel length, channel width and bias stress voltages at the drain and gate electrodes are presented. A semi-empirical HC degradation compact model is proposed, which is experimentally verified. The good accuracy of the degradation model makes it suitable for implementation in circuit simulation tools. The impact of the hot-carriers on a CMOS inverter is simulated using HSPICE.**

***Index Terms*—Degradation model, hot-carrier effect, n-FinFETs.**

I. INTRODUCTION

Fin-shaped field effect transistors (FinFETs) have been considered to be one of the most promising candidates for enabling to enhance the technology scalability by suppressing the short-channel effects (SCEs) due to better channel electrostatic control. Nevertheless, at very small device dimensions, the high electric fields imply hot-carrier (HC) degradation issues. The HC effect causes carrier trapping from the inversion layer into the gate dielectric bulk defects and interface state generation. These effects result in degradation of the transistor parameters (threshold voltage V_t, subthreshold swing coefficient η, effective carrier mobility μ_{eff}), which have a negative impact on the performance of analog and digital circuits.

Recently, we have developed an analytical compact model for the drain current of nanoscale FinFETs which has the unique feature of a unified charge-based expression for the drain current valid in all the regions of operation, which includes the device parameters V_t, η and μ_{eff} [1,2]. Thus, HC degradation modelling of the device parameters could lead to the prediction of the HC-related device degradation. In this paper, a semi-empirical HC degradation model based on the threshold voltage ΔV_t shift is developed, which is suitable for SPICE simulation of FinFET-based circuits. The performance degradation of the CMOS inverter is predicted based on this device model.

II. EXPERIMENTAL DETAILS

The HC experiments were performed on 5-fin n-channel SOI FinFETs with fin length L = 30 nm, fin height H_{fin} = 65 nm, fin width W_{fin} = 5, 10 and 15 nm, buried oxide thickness 145 nm, channel doping concentration 10^{15} cm^{-3} and TiN/HfO_2 gate insulator stack with equivalent gate oxide thickness t_{ox} = 1.7 nm.

In the HC experiments, the devices were stressed at room temperature by applying stress voltage to the drain and gate electrodes, with the other terminals grounded. In short-channel devices, it has been confirmed that the worst HC stress condition occurs at $V_{stress} = V_{ds} = V_{gs}$ [3]. The transfer characteristics were measured by using an Agilent B1500/1530 Semiconductor Device Analyzer. Based on the analysis of the transfer characteristics, the degradation of the threshold voltage V_t, the subthreshold ideality factor η and the on-state current were obtained.

III. SEMI-EMPIRICAL HOT-CARRIER DEGRADATION COMPACT MODEL

Fig. 1(a) shows the degradation of the transfer characteristics of a typical n-FinFET with L = 30 nm, W_{fin} = 10 nm, measured at V_d = 0.03 V after HC stress at V_{stress} = 1.8 V for different stress times. The degradation of the device parameters V_t, η and on-state drain current is clearly observed. The positive V_t shift indicates the built-up of a negative charge in the gate dielectric. The negative charge can result either from electron trapping in the gate dielectric or from generation of acceptor-type interface traps. Fig. 1(b) shows the transconductance g_m degradation during HC stress. Degradation of the maximum g_m is observed attributed to the interface degradation, with a simultaneous parallel g_m shift due to charge injection into the gate dielectric bulk defects over the entire short-channel length [4].

A. Degradation of the Threshold Voltage

The generated interface traps and the carrier trapping to bulk gate dielectric defects are directly linked to the threshold voltage change. Experimental data shows that the positive threshold voltage shift ΔV_t follows a time dependent power-law of the form:

$$\%\Delta V_t \propto t^n, \tag{1}$$

with the time power-law exponent n lying in the range of 0.19-0.2. In n-FinFETs it has been reported that n varies from 0.1 for pure charge injection into the gate dielectric bulk defects to 0.6 for pure interface trap generation [4]. The dependence of the V_t degradation on the stress voltage V_{stress}, for any bias stress conditions, follows the law:

$$\%\Delta V_t \propto \exp\left(c_1 V_{ds}\right), \quad (2)$$

The parameter c_1 extracted from experimental data is 3.95 V^{-1}.

Considering the dependence of the $\%V_t$ degradation on (V_{ds}-V_{gs}), the relationship between $\%\Delta V_t$ and stress voltages at the drain and gate can be generalized as:

$$\%\Delta V_t \propto \exp\left(c_1 V_{ds}\right)\exp\left[-c_2\left(V_{ds}-V_{gs}\right)\right], \quad (3)$$

The parameter c_2 extracted from experimental data is 1.6 V^{-1}.

The dependence of the $\%V_t$ degradation induced by HC stress on the reciprocal of the fin width $1/W_{fin}$, showed that the V_t degradation is independent on the fin width of the investigated devices.

The dependence of the $\%V_t$ degradation induced by HC stress on the reciprocal of the channel length 1/L follows the power-law relationship between $\%\Delta V_t$ and 1/L:

$$\%\Delta V_t \propto \left(1/L\right)^b, \quad (4)$$

where b = 3.2 indicating that the channel length plays important role on HC degradation unlike the fin width. The dependencies denoted in (1)-(4) are verified by experimental data. Thus, for the n-FinFETs of the present technology, the HC-induced $\%V_t$ degradation model can be expressed as:

$$\%\Delta V_t = Ct^n\left(1/L\right)^b \exp\left(c_1 V_{ds}\right)\exp\left[-c_2\left(V_{ds}-V_{gs}\right)\right], \quad (5)$$

where C = 280 is a constant related to the specific FinFET technology, extracted from the experimental data.

B. Degradation of the Effective Electron Mobility

Fig. 2(a) shows plots of the drain current (I_{ds}) versus gate overdrive ($V_{gs} - V_t$) of n-FinFET with W_{fin} = 10 nm, measured at V_{ds} = 0.03 V after HC stress at V_{stress} = 1.8 V for different stress times. The on-state current in the linear region is degraded indicating reduction of the carrier mobility due to the HC-induced traps. An empirical formula has been derived to describe the impact of the interface traps in the transistor inversion region on the effective electron mobility $\mu_{eff,o}$ of the fresh device through the threshold voltage shift ΔV_t [5]:

$$\mu_{eff} = \frac{\mu_{eff,o}}{1+\alpha_1 \Delta V_t}, \quad (6)$$

where α_1 is process dependent mobility degradation parameter. Considering the impact of the generated interface traps on the effective electron mobility, the drain current of the fresh device I_{dso} is written as:

$$I_{ds} = \frac{I_{dso}}{1+\alpha_1 \Delta V_t}, \quad (7)$$

Equation (7) was verified for a FinFET with L = 30 nm and W_{fin} = 10 nm, stressed at V_{stress} = 1.8 V using the parameter α_1 = 1 V^{-1}. As shown in Fig. 2(b), the model results are in good agreement with the experimental results.

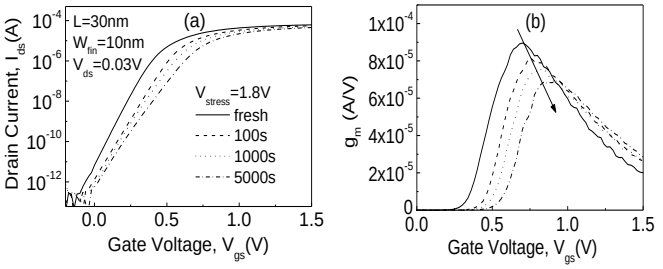

Fig. 1 (a) I_{ds}-V_{gs} characteristics and (b) g_m degradation before and after stress at V_{stress} = 1.8 V for different stress times.

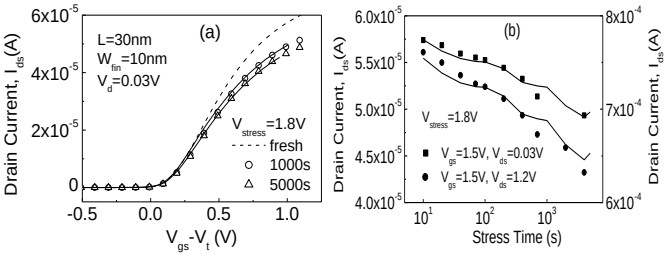

Fig. 2 (a) Drain current I_{ds} versus gate overdrive (V_{gs}-V_t) before stress and after stress at V_{stress} = 1.8 V for different stress times. (b) Evolution of the drain current, measured at V_{gs} = 1.5 V and V_{ds} = 0.03 and 1.2 V, with stress time of the device stressed at V_{stress} = 1.8 V. The symbols correspond to the experimental data and the lines to the model (7) using the parameter $\alpha_1 = 1V^{-1}$.

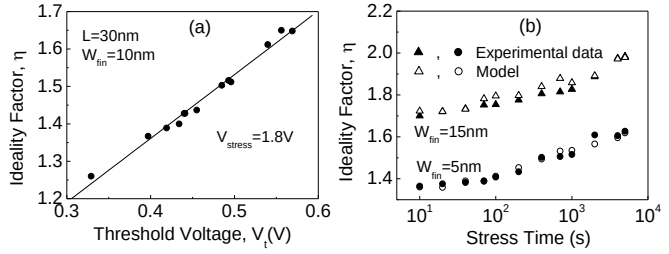

Fig. 3 (a) Relationship between ideality factor and threshold voltage of a device after stress at V_{stress} = 1.8 V. (b) Dependence of the ideality factor η with stress time of FinFETs with L = 30 nm and different W_{fin} by modeling η with (8).

C. Degradation of the Subthreshold Swing Coefficient

The subthreshold swing coefficient η and the threshold voltage V_t of the HC stressed devices are linearly correlated as shown in Fig. 3(a).

Thus, the degradation of the parameter η as a function of the threshold voltage shift ΔV_t can be modelled by the empirical formula:

$$\eta = \eta_o\left(1+\alpha_2 \Delta V_t\right), \quad (8)$$

where η_o is the subthreshold swing coefficient of the fresh device and α_2 is the process dependent subthreshold swing coefficient degradation parameter. The degradation of the experimental η with stress time for FinFETs with fin widths W_{fin} = 5 nm and 15 nm is presented in Fig. 3(b). Equation (8) has been verified using α_2 = 1.2 V^{-1} for the n-FinFETs of the present technology.

Combining (5)-(8) and the compact model of [4], the impact of the HC effect on the device performance can be predicted. Fig. 4 presents the experimental transfer characteristics of FinFETs with W_{fin} = 5 and 10 nm, channel lengths L = 30 and

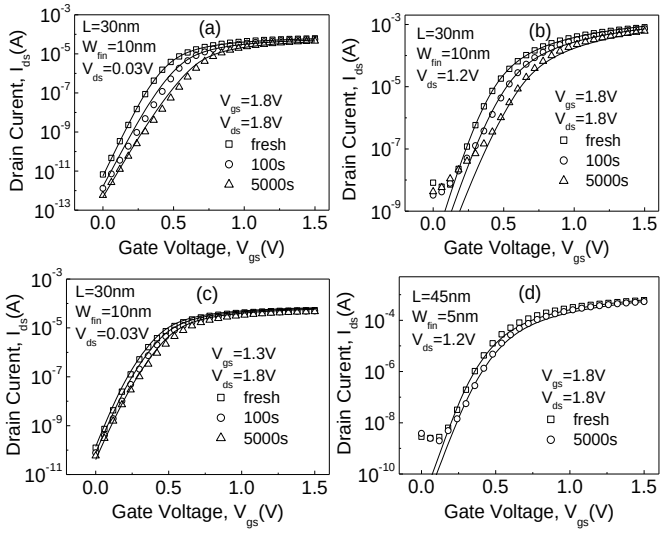

Fig. 4 Experimental (symbols) and model (lines) transfer characteristics before and after stress at different stress bias and stress time conditions of FinFETs, using the model parameters of the fresh devices: (a), (b) V_E = 0.1 V, μ_o = 120 cm^2/Vs, θ_o = 0.3, (c) V_E = 0.1 V, μ_o = 157 cm^2/Vs, θ_o = 0.3, (d) V_E = 0.14 V, μ_o = 161 cm^2/Vs, θ_o = 0.05.

45 nm, stressed at different bias voltages and for different stress times. As shown in Fig. 8, the agreement between the experimental and modelled results is good, supporting the validity of the proposed HC compact model.

IV. IMPACT OF HC DEGRADATION ON CIRCUIT PERFORMANCE

The proposed HC degradation model has been integrated in the analytical drain current compact model of nanoscale FinFETs [4], coded using Verilog-A description language which is readily available in the HSPICE circuit simulator. Our goal is to compute the impact of hot-carriers on the aging of the n-FinFET under the specific stress conditions dictated by the operation of the CMOS inverter. The device parameters are: W_{fin} = 10 nm, H_{fin} = 65 nm, t_{ox} = 1.7 nm, L = 30 nm, doping concentration of silicon channel $N_A = 10^{15}$ cm^{-3}, doping concentration of the source/drain contacts $N_D = 10^{20}$ cm^{-3} and electron mobility μ_0 = 120 cm^2/Vs.

The general decrease of the drain current characteristic due to HC degradation mainly affects the gate switching delay. This aging effect cumulatively builds up over prolonged periods, resulting in performance degradations that may eventually lead to unacceptably large delay values. The degradation of the saturation drain current of a transistor due to HC effects is directly related to the age function defined as:

$$age\left(V_{gs},V_{ds},\Delta V_t,t\right)=t/\tau\left(V_{gs},V_{ds},\Delta V_t\right)=R\left(V_{gs},V_{ds},\Delta V_t\right)\times t\,, \quad (9)$$

where τ is the device lifetime and R is the rate of aging over time. Solving (5) with respect to stress time results the device lifetime τ, which is a function of the stress bias voltages (V_{gs}, V_{ds}) and the threshold voltage degradation value ΔV_t. Hence, by defining $\%\Delta V_t$ reaching some value DT as the end of the device life, the lifetime τ is given by:

$$\tau=\sqrt[n]{\frac{DT\cdot L^b}{C}e^{-c_1V_{ds}+c_2\left(V_{ds}-V_{gs}\right)}}\,, \quad (10)$$

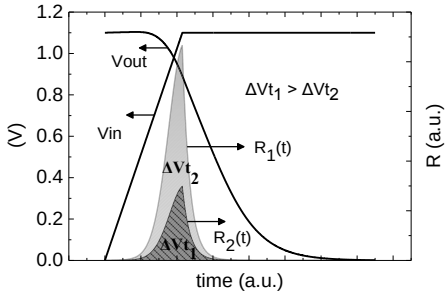

Fig. 5 Transient response of R(t) with different ΔV_t values for the n-FinFET device during a rising switching event at the input of the CMOS inverter.

Apparently, the device lifetime can be defined differently depending on the application. An arbitrary circuit may impose a tighter threshold voltage degradation tolerance DT to avoid operation failure.

We focus our study on the n-FinFET of the CMOS inverter. The inverter operation for which there is a sufficient number of carriers in the channel of the n-FinFET corresponds to the rising input switching state only, specifically when the device is saturated. The propagation delay of this switching state is completely defined by the driving current of the n-type device. During this operation, the defect generation rate is time-varying R(t) as the device is biased at different voltages in each time step. HC effects do not experience recovery effects and the application of HC stress results in monotonous aging. By taking into account this property, a term called age gain (AG) per transition of a MOSFET can be introduced. The aging of a device is the sum of device age gains per signal transition [6]:

$$age=\sum_{all\ trans}AG\,, \quad (11)$$

The device AG over each transition period is defined with the integral of the aging rate function R(t):

$$AG=\int_{trans}R\left(t,\Delta V_t\right)dt\,, \quad (12)$$

This integral computes the age gain associated with one specific transition and uses the quasi static approach to approximate the integral as a finite sum.

In the CMOS inverter, the bias conditions under which the n-FinFET transistor switches depend on the input rise time tau, the capacitive load C_L and the supply voltage V_{DD}. The aging rate function R(t) being bias dependent, varies its waveform respectively under different circuit operating conditions. Furthermore, because R(t) is defined as the inverse of the device lifetime τ, different definitions of τ lead to different R(t) waveforms for a given operating condition. We remind that τ is correlated with the threshold voltage degradation tolerance ΔV_t. Fig. 5 plots the rate of aging R(t) = $1/\tau$(t) of the n-FinFET device of an inverter under the same operating conditions (tau, C_L and V_{DD}) with different lifetime definitions $\tau_1(\Delta V_{t1})$ and $\tau_2(\Delta V_{t2})$. The responses are taken during the switching event of the inverter with a rising input ramp. Obviously, the plot with the lifetime corresponding to the lower ΔV_t value ($\Delta V_{t1}>\Delta V_{t2}$) has a larger AG value as

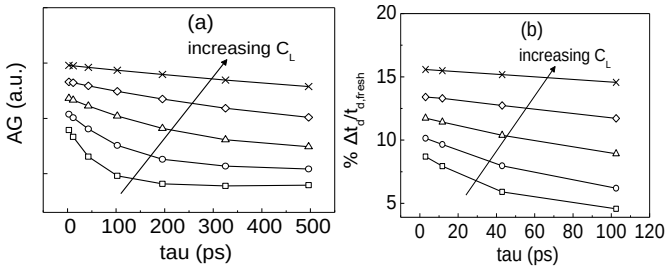

Fig. 6 (a) The age gain (AG) value as a function of the input transition time tau for different capacitive loads C_L. (b) The inverter delay degradation $\%\Delta t_d$ versus rising input transition tau, under different capacitive loads.

fewer transitions are needed to degrade the corresponding threshold voltage. The number of transitions needed for a defined degradation of V_t depends on the AG per transition and is calculated as $N_{tran} = 1/AG$.

Fig. 6(a) shows the n-FinFET age gain dependency on the rising input transition time of the inverter for different capacitance loads. ΔV_t is kept constant at an arbitrary value for every corner. We observe that smaller input transition times and larger capacitances increase the age gain for a constant threshold degradation value. Furthermore, the dependence of the AG on the input transition time follows the corresponding dependence of R_{peak} which is opposite to that of the saturation time interval $t_{n,sat}$. The reason is that the rate at which R_{peak} decreases outmatches the rate at which $t_{n,sat}$ increases, when the input transition time increases for a given capacitance load.

From a physical point of view, the form of the plots in Fig. 6(a) is explained by the fact that HC degradations are caused by the charge carriers flowing through the channel and larger load C_L requires more charge to move, while smaller transition tau makes the carriers to move faster, thus causing more damage. The results shown in Fig. 6(a) are now projected on the degradation of the cell delay. Fig. 6(b) plots the curves for the inverter delay degradation $\%\Delta t_d$ versus rising input transition, under different load capacitances. Unlike the plot in Fig. 5, the age gain of each corner is tied to the largest age gain. That is the one with the faster input transition and the larger capacitive load. For this purpose, the threshold voltage degradation value ΔV_t of each other corner is reduced more or less, depending on the initial age gain difference. Consistent to the results shown in Fig. 6(a), the variations of the gate delay in Fig. 6(b) follow the same trends.

HC effects can slow down the signal transition during the aging process, which in turn reduces the age gain per transition further, slowing down the HC-based circuit aging. Therefore, in principle, the circuit delay degradation is generally a decelerating process. It has been demonstrated that this deceleration effect of aging is quite insignificant and can safely be ignored [6].

V. CONCLUSION

The HC degradation mechanisms in nanoscale n-FinFETs were investigated under different stress conditions, including interface degradation and hot carriers injection into the gate dielectric. The impact of degradation on the device parameters (threshold voltage, subthreshold swing coefficient, effective carrier mobility) has been expressed with empirical formulas for the devices of the specific FinFET technology. A semi-empirical compact model is proposed to predict the device performance degradation, which aggress well with the experimental date in all operation regimes. Finally, a CMOS inverter is simulated to predict its performance degradation due to HC stress.

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REFERENCES

[1] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, K. Papathanasiou, J. Jomaah, and G. Ghibaudo, "Analytical unified threshold voltage model of short-channel FinFETs and implementation," *Solid-State Electron* , vol. 64, pp. 34-41 (2011).

[2] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, I. Pappas, K. Papathanasiou, C. A. Dimitriadis, M. Bucher, and G. Ghibaudo, "Compact model of drain current in short-channel triple-gate FinFETs," *IEEE Trans. Electron Devices*, vol. 59, pp. 1891-1898 (2012).

[3] S.-Y Kim and J. H. Lee, "Hot carrier-induced degradation in bulk FinFETs," *IEEE Electron Dev. Lett.*, vol. 26, pp. 566-568 (2005).

[4] M. Cho, P. Roussel, B. Kaczer, R. Degraeve, J. Franco, M. Aoulaiche, T. Chiarella, T. Kauerauf, N. Horiguchi, and G. Groeseneken, "Channel hot carrier degradation mechanism in long/short channel n-FinFETs," *IEEE Trans. Electron Dev.*, vol. 60, pp. 4002-4007 (2013).

[5] E. Maricau, P. De Wit, and G. Gielen, "An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog IC applications," *Microelectron. Rel*., vol. 48, pp. 1576-1580 (2008).

[6] Jianxin Fang and Sachin S. Sapatnekar, "The Impact of Hot Carriers on Timing in Large Circuits," Proceedings of the Asia-South Pacific Design Automation Conference, pp. 591-596, 2012.