CMOS Digital Gate Pre-Characterization Using Equivalent Inverters

Ch. Galani, A. Tsormpatzoglou, I. Messaris, M. Ntogramatzi, N. Karagiorgos, S. Goudos, S. Nikolaidis
Department of Physics
Aristotle University of Thessaloniki
54124, Thessaloniki, Greece
snikolaid@physics.auth.gr

***Abstract*—In this paper, an alternative approach for performing the pre-characterization of CMOS digital gates is proposed. This method aims to eliminate the use of circuit simulators like HSPICE during the cell pre-characterization in order to accelerate it. This procedure is necessary for the operation of technology models such as CCS, NLDM and NLPM. This is achieved by employing an analytical inverter model along with an equivalent inverter model taking advantage of the fact that digital gates can be reduced to equivalent inverter circuits. The inverter models used in this work as well as the technology requirements are briefly described. Results validate the accuracy of the proposed procedure.**

Keywords—Cell characterization; Gate modeling; Equivalent inverter; timing analysis; simulation;

I. INTRODUCTION

When simulating the operation of a circuit, the accuracy and speed of calculations are just as important. For that reason the trade-off between those two properties defines the method to be used for simulation and cell characterization. Especially when dealing with large digital circuits a small sacrifice in accuracy on timing and power analysis is permissible in order to achieve higher simulation speed. Three technology models that follow this principle are (a) CCS model (Composite Current Source) [1] for cell timing and power analysis, (b) NLDM (Non-Linear Delay Model) for timing analysis and (c) NLPM (Non-Linear Power Model) for power analysis. These models perform timing and power analysis much faster and slightly less accurately than other SPICE like circuit simulators

These models need as input a certain set of values that must be organized in a specific arrangement and be provided in the form of a .lib type file. In order to produce a .lib type file, a cell pre-characterization procedure needs to take place. The results of this procedure are the values of the electrical quantities necessary for the operation of the timing and power analysis model which are obtained from simulation and are unique for each transistor technology.

Simulators like HSPICE, being very precise, present a slow production rate of the aforementioned electrical values and hence using this tool is extremely time consuming especially if the cells of a whole library need to be pre-characterized. For the acceleration of this procedure the approach applied here uses an analytical inverter model and an equivalent inverter model. The idea is to strip down every digital gate cell to an equivalent inverter based on the grounds that the electrical behavior of the gates can be derived from results obtained for inverters [2]. In the work proposed here, a PTM (Predictive Technology Model) BSIM model (Berkeley Short-channel IGFET Model) is used for the bulk 45nm transistor technology. The studied cells are part of the Nangate Open Cell Library PDK (Process Design Kit) v.1.3.2010. Specifically the pre-characterization procedure has been conducted for the gates: Inverter, two-input NAND and NOR.

II. INVERTER BASED MODELING

A. CMOS Inverter

The Inverter model for nano-scale technologies [2] used in this work provides results regarding propagation delay and power consumption both dynamic and static. This analytical inverter model uses a modification of the transistor current model that includes nano-scale effects such as DIBL (Drain Induced Barrier Lowering), CLM (Channel Length Modulation) and NWE (Narrow Width Effect). Furthermore the sub-threshold current of the transistor when operating in the cut-off region is also included along with the influence of the drain-to-bulk capacitance of both transistors on the output voltage waveform.

The advantage of the modified expressions of the transistor current used is that they are not complex and therefore easy to handle. The values assigned to the equation parameters were derived using a fitting procedure. As far as the output voltage is concerned, the differential equation which describes the inverter circuit operation can be found by applying Kirchhoff's current law at the output node. The operation of the inverter is divided into regions according to the regions of operation of the transistors. Solving the aforementioned differential equation for each region of operation of the inverter provides the form of the output voltage curve.

B. Equivalent Inverter

In order to avoid using mathematical methods to model more complex digital gates since it is a challenging task, especially for nano-scale technologies, the equivalent inverter approach follows another principle. It takes advantage of the great number of analytical methods already proposed for describing the operation of the CMOS inverter and aspires to replace digital gates with an equivalent inverter using macromodeling methods.

The aim is to accurately simulate the operation of CMOS digital gates using equivalent inverters under the same input conditions regarding temperature (T), the width of the nMOS transistor of the original gate (W_n), the supply voltage (V_{DD}), the input ramp transition time (τ), and the output load capacitance (C_{out}). To achieve that, the suitable widths of the equivalent inverter transistors are measured through a simulation procedure using HSPICE for every input parameter combination and for each gate. After the extraction of the equivalent widths an equation is constructed using fitting techniques. As a result the equivalent width is expressed as a function of the input conditions:

$$W_{eq} = f(temp, W_n, V_{dd}, tau, C_L) \quad (1)$$

One equation corresponds to one input pin of the gate and one type of the input voltage transition which is either rising or falling.

III. MODEL REQUIREMENTS

The cell pre-characterization necessary for the CCS, NLDM and NLPM models was performed using the previous mentioned inverter models. In order to accelerate the process, these models were implemented in C^{++} code. The parameters that are given as input to the C^{++} code are given in Table 1.

Table 1: C++ input parameters

Circuit temperature	*Temp*
Width of the nMOS transistor	W_n
Supply voltage	V_{dd}
Transition time of input ramp	*Tau*
Output load	C_L
Type of input voltage ramp	Rising/Falling

Under the instructions of the timing/power analysis technology only one input of the logic gate changes its value at a certain time space and all of the rest inputs are tied to steady voltages thus the switching activity is limited to only one input.

The minimum and maximum value of C_{out} and τ cover a wide range. For that reason the model requires that measurements are conducted for 7 specific values of output load and an equal number of input transition time values. These values are produced by a number generator program which uses a distribution of equal size logarithmic steps [1]. The resulting 49 combinations of these values define the design corners. The values of the other input parameters range according to the transistor technology used and the gate topology. All the corner values as well as the range of the other input parameters are given in Table 2.

Table 2: Input parameter values

nMOS transistor width: $\boldsymbol{W_n}$ (nm)(range)	100 – 415
Supply Voltage: $\boldsymbol{V_{dd}}$(V)(range)	0.7 – 1.25
Input transition time: *tau* (ps)	2.9, 12, 43, 102, 195, 325, 496
Load capacitance: $\boldsymbol{C_L}$ (fF)	0.37, 1.9, 3.8, 7.6, 15.1, 30.3, 60.6
Temperature: *temp* (°C)(range)	0 – 125

The execution of the C^{++} code produces a .lib file, compatible with the technology model requirements. For each value of supply voltage and temperature a different .lib file is produced which includes the remaining input parameterization. This file contains the values of the electrical quantities that are needed for the cell characterization. These values are divided into two categories, those concerning the time response of the gate and those concerning power consumption, either dynamic or static. Furthermore the CCS, NLDM and NLPM technology models are comprised of two separate models, one for the description of the behavior of a cell when it is driving another gate and one for when it is driven by another gate. In the paragraphs that follow the electrical quantities produced by the .lib file are briefly mention. An extensive description can be found in [1]

Concerning timing analysis the electrical quantities needed are the output voltage propagation delay and transition time as a function of **t**au and C_L , when the cell is used to drive other gates**.** The transition time is defined as the interval between the time points when the output reaches the 30% and 70% of the supply voltage. The output current waveform is also needed and it is produced by multiplying C_L with the output voltage derivative. When the cell is viewed as an output load, the value of its capacitance needs to be defined. Furthermore, concerning power analysis the .lib file provides the necessary values of static and dynamic current or power depending on the specific requirements of the model used.

IV. RESULTS

In Table 3 the average errors of the quantities $t_{VDD/2}$ and $I_{integral}$ between results from simulation, conducted using HSPICE, and the model for V_{DD}=1.1V and temp=25°C are presented. The time $t_{VDD/2}$ refers to the output voltage waveform, when the supply voltage reaches the 50% of its value and $I_{integral}$ is the integral of the current waveform of the conducting block of transistors for each gate. We separate 4 cases of operation concerning the input pin and the transition type of the input voltage ramp. Note that A1 refers to the input pin of the transistor closer to the output of the gate.

Table 3: Simulation and model comparison

Gate	Case	$t_{VDD/2}$	$I_{Integral}$
Inverter	Rising	2.1 %	6.3%
NAND	A1 Falling	2.6%	5.8%
NOR	A1 Rising	2%	6.2%

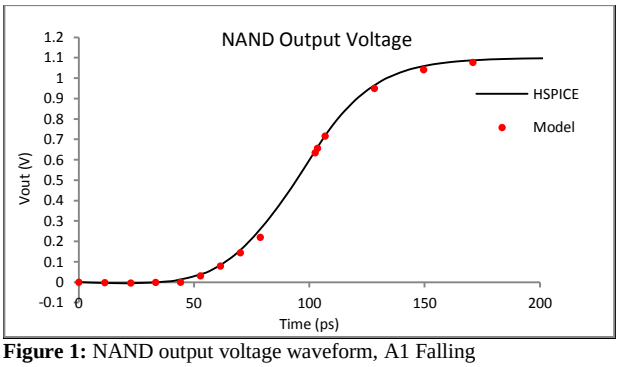

Figure 1: NAND output voltage waveform, A1 Falling

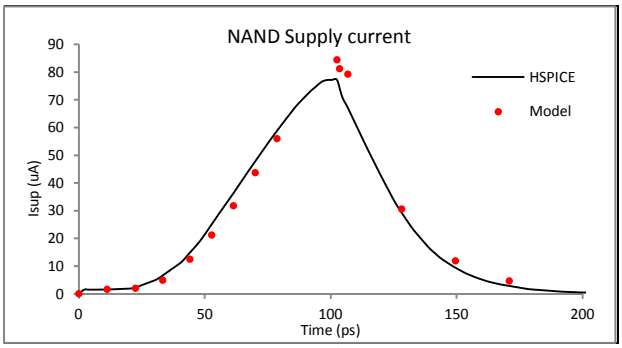

Figure 2: NAND supply current waveform, A1 Falling

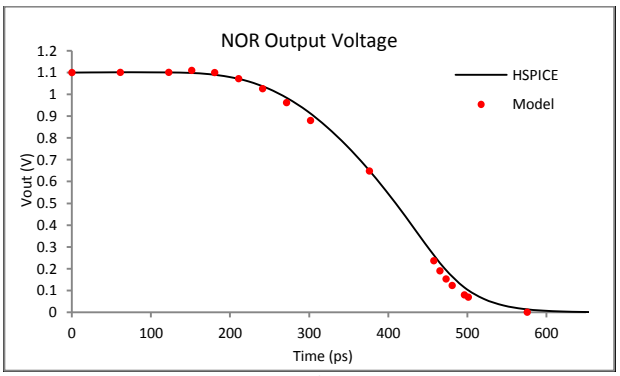

Figure 3: NOT output voltage waveform, A1 Rising

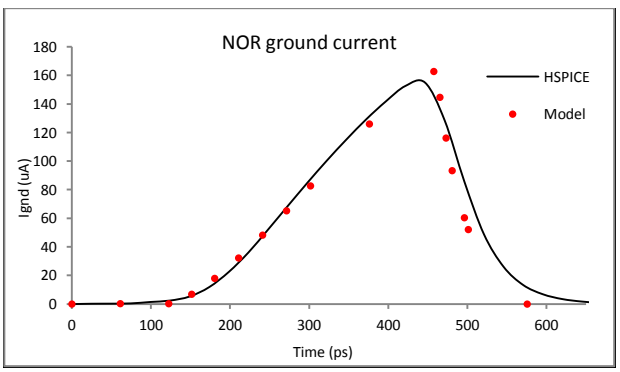

Figure 4: NOR ground current, A1 Rising

For the same input corners, Figures 3 and 4 show the output voltage waveform and ground current respectively for gate NOR, case A1 Rising. On Figures 1 and 2 the output voltage waveform and supply current waveform are illustrated for case A1 Falling, W_n=175nm, V_{DD}=1.1V, tau=103ps, C_L=3.79fF and temp=25°C.

V. Conclusions

In this paper an alternative method for performing CMOS cell pre-characterization is presented. In order to avoid using a circuit simulator for this procedure a CMOS inverter model and an equivalent inverter model for replacing CMOS gates were used. These models were embodied in a C^{++} code which produces a .lib type file that contains all the necessary information needed by technology models such as CCS, NLDM and NLPM in order to perform timing and power analysis. For the evaluation of this model 3 gates were used, an inverter, two-input NAND and NOR gates. Results verify the accuracy of the model.

Acknowledgment

This work was supported by Hellenic Funds and by the European Regional Development Fund (ERDF) under the Hellenic National Strategic Reference Framework (ESPA) 2007-2013, according to Contract no. 11ΣΥΝ_5_719 project NANOTRIM.

References

[1] CCS Timing, Technical White Paper, Version 2, Synopsys, Inc., Dec.2006,http://www.opensourceliberty.org/ccspaper/ccs_timing_wp.pdf

[2] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, "*Digital Integrated Circuits: A Design Perspective*" , 2 ed., Prentice Hall Electronics and VLSI Series, Upper Saddle River, NJ: Prentice Hall/Pearson Education, 2003

[3] P. Haourani, S.Nikolaidis, "A Unified CMOS Inverter Model for Planar and FinFET Nanoscale Technologies" IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) 2014.

[4] Nangate 45 nm Open Cell Library, Version 1.3, Nangate Inc., Jul. 2009.[Online].Available: http://www.si2.org/openeda.si2.org/projects/nangatelib.

[5] Predictive Technology Model (PTM), http://www.eas.asu.edu/ptm